INFORMATION REDACTED PURSUANT TO THE FREEDOM OF INFORMATION ACT (FOIA), 5 U.S.C. 552(B)(6)

[redacted]

Master's Degree Course in
**Mechatronic Engineering**

Master's Degree Thesis

# Control Board Design for Dual Voltage Source Inverters in Automotive Applications

**Supervisors**

[redacted]

**Candidate**

[redacted]

October 2024

# Summary

The work presented in this thesis is part of the European HiEFFICIENT project, which aims to push the boundaries of powertrain inverter design, by enhancing energy efficiency, reducing costs, and promoting the adoption of electric mobility and green energy systems.

In this context, Ideas & Motion (I&M), the hosting company for this thesis, is responsible for the complete design, development, and prototyping of an automotive-grade modular traction inverter with an integrated control unit.

This thesis addresses the design and development of a prototype control board with a modular and flexible architecture, emphasizing both safety and adaptability.

The modularity of the design allows the control unit to drive either single or dual Voltage Source Inverters (VSI), providing scalability for different powertrain configurations. It also supports 3-level (3L) inverter topologies by generating up to 18 PWM control signals.

To ensure the safety and reliability of the electrical vehicle, the design incorporates several protection mechanisms, such as reverse polarity and battery short-circuit protection, along with redundancy through dual power supply compatibility, ensuring uninterrupted operation in the event of a power source failure. The control board also includes hardware safety logic and an overcurrent detection circuit to enable fast response times and prevent potential system damage.

To further enhance adaptability, the board interfaces with position sensors from two motors, supporting both analog and digital types. Additionally, it is equipped to handle multiple communication protocols, including SSI, SENT, CAN, and Ethernet, ensuring robust, high-speed communication and reliable data exchange for control operations and system diagnostics.

To improve the board's versatility and integration into various systems, it provides programmable analog and digital inputs, as well as high-side and low-side outputs, enabling seamless interfacing and management of several external auxiliary systems.

Simulations of each circuit design were conducted using specific device models to ensure accuracy and full compliance with the application. These simulations allowed for the evaluation of various design solutions, selecting the best approach in terms of performance and cost.

Finally, experimental validation was performed on the most critical circuits, demonstrating the good performance of the control board under real-world conditions.

This thesis presents a control board design that effectively combines modularity, safety, and adaptability through theoretical design, simulation, and experimental validation. the resulting board provides a high-performance, versatile solution for the design and implementation of traction inverter control boards, addressing the rigorous requirements of modern electric vehicle powertrains.

# Acknowledgements

I would like to express my sincere gratitude to the management and staff of Ideas & Motion for providing me with the opportunity to conduct this thesis. I especially want to thank [redacted] for his invaluable assistance, continued support and guidance throughout the project. I would also like to thank Professor [redacted] for his availability and support during this work.

# Contents

**List of Figures** VII

**List of Acronyms** X

**1 Introduction** 1
1.1 Scope of the Thesis . . . . . 1
1.2 Thesis Framework . . . . . 2
1.3 Organization of the Thesis . . . . . 2

**2 Traction Inverter** 3
2.1 Main Components . . . . . 4
2.2 Three Level Inverters . . . . . 8
2.3 I&M Voltage Source Inverter . . . . . 9

**3 Control Board** 12
3.1 Main Features . . . . . 12
3.2 Design and Testing Tools . . . . . 15

**4 Power Supply** 17
4.1 External Supply . . . . . 18
4.2 On-Board PMIC . . . . . 19
4.3 Power Consumption Estimation . . . . . 21
4.3.1 Derivation of Pre-Regulator Total Power Losses . . . . . 22
4.3.2 Thermal Considerations . . . . . 24

**5 Analog Position Sensors** 25
5.1 Overview . . . . . 25
5.2 Conditioning Circuit Design . . . . . 27
5.2.1 Filter Design . . . . . 30
5.3 Simulation . . . . . 33
5.4 Testing . . . . . 36

**6 Digital Position Sensors** 41
6.1 Overview . . . . . 41
6.2 Conditioning Circuit Design . . . . . 42
6.3 Simulation . . . . . 44
6.4 Testing . . . . . 47
6.5 Synchronous Serial Interface . . . . . 49

**7 Programmable Inputs** 51
7.1 Shift Registers . . . . . 51
7.2 Rereading Pull-Up Voltage . . . . . 54
7.3 Pull-Select From MCU . . . . . 56
7.4 Single Edge Nibble Transmission . . . . . 58

**8 Safety Features** 61
8.1 Overcurrent Detection . . . . . 61
8.2 Latch . . . . . 63
8.3 Overvoltage Detection . . . . . 64
8.4 Hardware Safety Logic . . . . . 66
8.5 Simulations . . . . . 68
8.6 Testing . . . . . 71

**9 SPI Level Shifter** 74
9.1 MOSFET-Based Level Shifter . . . . . 75
9.2 Simulations . . . . . 76

**10 PCB Design** 80

**11 Conclusions** 82

**Bibliography** 84

**A Power Consumption Spreadsheet** 87

# List of Figures


1 *Schematized view of an inverter system within an EV powertrain.* . 4
2 *Line to line voltage and current of a 2L-VSI (a) and 3L-NPC (b) [1].* 9
3 *Complete inverter design showing the dual voltage source implementation.* . . . . . 9
4 *Exploded view of the inverter design showing control, driver, and power boards, including current sensing PCB.* . . . . . 10
5 *Enclosure of the single inverter design.* . . . . . 11

6 *Overview of the control board architecture* . . . . . 12
7 *Table with test equipment used.* . . . . . 16

8 *Power Supply Scheme of the Control Board.* . . . . . 17
9 *Table of outputs with nominal voltage, max current, and comments.* 20
10 *Plot of the total power losses of the TLF35584 pre-regulator.* . . . . 23

11 *Circuit diagram showing the adopted solution for conditioning single-ended and differential analog position sensor signals.* . . . . . 27
12 *Circuit diagram showing the adopted solution for conditioning the SinCos differential input signals.* . . . . . 28
13 *LTspice scheme of the differential SinCos conditioning circuit.* . . . 34
14 *Frequency domain simulation result.* . . . . . 34
15 *Time domain simulation results with 1 kHz input frequency.* . . . . 35
16 *Time domain simulation results with 25 kHz input frequency.* . . . . 36
17 *Oscilloscope capture at 1 kHz input frequency; on the upper graphic differential inputs, on the lower graphic the output of the adder and the ADC input.* . . . . . 37
18 *Oscilloscope capture at 25 kHz input frequency; on the upper graphic differential inputs, on the lower graphic the output of the adder and the ADC input.* . . . . . 38
19 *Frequency response measured with Analog Discovery 2: Blue curve shows full circuit, yellow curve shows first filtering stage.* . . . . . 39

20 *Six-Step Motor Commutation Control Scheme for a PMSM motor with one pole-pair [2].* . . . . . 41
21 *Circuit diagram showing the adopted solution for conditioning the digital position input signals.* . . . . . 42
22 *LTspice scheme of the digital position conditioning circuit.* . . . . . 45
23 *Time domain simulation results with 1 kHz input frequency.* . . . . 45
24 *Frequency domain simulation results.* . . . . . 46
25 *Frequency response measured with Analog Discovery 2: Blue curve shows full circuit, yellow curve shows first filtering stage.* . . . . . 47
26 *Oscilloscope capture at 1 kHz input frequency.* . . . . . 48
27 *Oscilloscope capture of rising and falling edge delay measurements.* . 48
28 *SSI transceiver logic diagram [3].* . . . . . 50

29 *Shift Register Internal Diagram [4],* . . . . . 52
30 *SPI timing diagram showing clock behavior for different CPOL and CPHA configurations [5].* . . . . . 53
31 *Circuit diagram showing the flexible input "ReReading Pull-Up Voltage".* . . . . . 54
32 *Circuit diagram showing the flexible input "Pull-Select from Micro"* 57
33 *Circuit diagram showing the flexible input "Sent".* . . . . . 59

34 *Circuit diagram showing the adopted solution for the overcurrent detection.* . . . . . 62
35 *Circuit diagram showing the adopted solution for the latch using a comparator with a diode on the feedback.* . . . . . 63
36 *Circuit diagram showing the adopted solution for the Overvoltage detection.* . . . . . 64
37 *Inverting comparator with hysteresis.* . . . . . 65
38 *Circuit diagram showing the adopted solution for the hardware safety logic.* . . . . . 67
39 *LTspice scheme of the Overcurrent, Overvoltage, and Latch circuits.* 69
40 *Time domain simulation results for the overcurrent detection circuit.* 69
41 *Time domain simulation results for the overvoltage detection circuit.* 70
42 *Oscilloscope capture of the overcurrent detection circuit.* . . . . . 71
43 *Overcurrent response delay test results.* . . . . . 72

44 *Circuit diagram showing the adopted solution for the MOSFET-based level shifter.* . . . . . 75
45 *LTspice scheme of the level shifter based on resistive voltage divider.* 77
46 *Time domain simulation results with 100 kHz, 1 MHz, and 10 MHz input frequencies.* . . . . . 77
47 *LTspice scheme of the level shifter based on MOSFET using NX3008NBKS.* . . . . . 78

48 *Time domain simulation results with 100 kHz, 1 MHz, and 10 MHz input frequencies - MOSI line.* . . . . . 78
49 *Time domain simulation results with 100 kHz, 1 MHz, and 10 MHz input frequencies - MISO line.* . . . . . 79

50 *Control board top layer placement* . . . . . 81

# List of Acronyms

**3L-NPC** Three Level Neutral Point Clamped.

**AC** Alternating Current.

**ADC** Analog to Digital Converter.

**ANPC** Active Neutral Point Clamped.

**ASC** Active Short Circuit.

**ASIL** Automotive Safety Integrity Level.

**BLDC** Brushless DC Motor.

**BMS** Battery Management System.

**BOM** Bill Of Materials.

**CAN** Controller Area Network.

**CLK** Clock.

**CPHA** Clock Phase.

**CPOL** Clock Polarity.

**CPU** Central Processing Unit.

**CRC** Cyclic Redundancy Check.

**CS** Chip Select.

**DC** Direct Current.

**DSP** Digital Signal Processing.

**ECU** Electronic Control Unit.

**EM** Electrical Machine.

**EMC** Electromagnetic Compatibility.

**EMF** Electromotive Force.

**EMI** Electromagnetic Interference.

**EV** Electric Vehicle.

**F-RAM** Ferroelectric Random Access Memory.

**GND** Ground.

**GTM** Generic Timer Module.

**HV** High Voltage.

**HVIL** High Voltage Interlock Loop.

**HW** Hardware.

**I/O** Input/Output.

**I&M** Ideas & Motion S.r.l..

**IC** Integrated Circuit.

**IGBT** Insulated Gate Bipolar Transistor.

**IM** Induction Motor.

**ISA** Instruction Set Architecture.

**LDO** Low Dropout.

**LUT** Lookup Table.

**LV** Low Voltage.

**MCU** Microcontroller Unit.

**MISO** Master In Slave Out.

**MOSFET** Metal-Oxide Semiconductor Field-Effect Transistor.

**MOSI** Master Out Slave In.

**MSB** Most Significant Bit.

**NTC** Negative Temperature Coefficient.

**OEM** Original Equipment Manufacturer.

**OP-AMP** Operational Amplifier.

**OTA** Over The Air.

**OV** Over Voltage.

**PCB** Printed Circuit Board.

**PHM** Prognostic Health Management.

**PM** Permanent Magnet.

**PMIC** Power Management Integrated Circuit.

**PMSM** Permanent Magnet Synchronous Machine.

**PN** Part Number.

**PWM** Pulse Width Modulation.

**RC** Resistor-Capacitor.

**RCLK** Register Clock.

**RISC** Reduced Instruction Set Computer.

**RMS** Root-Mean-Square.

**RPM** Revolution Per Minute.

**RPS** Revolution Per Second.

**SENT** Single Edge Nibble Transmission.

**SER** Serial Input.

**SME** Small Medium Enterprise.

**SPDT** Single Pole Double Throw.

**SPI** Serial Peripheral Interface.

**SRCLK** Shift Register Clock.

**SRM** Switched Reluctance Motor.

**SS** Safe State.

**SSI** Synchronous Serial Interface.

**SW** Software.

**THD** Total Harmonic Distortion.

**TTL** Transistor Transistor Logic.

**UART** Universal Asynchronous Receiver-Transmitter.

**UV** Under Voltage.

**Vbatt** Battery Voltage Level.

**VBD** Voltage Battery Direct.

**VBDaux** Voltage Auxiliary Battery.

**VBP** Voltage Battery Protect.

**Vgs** Gate-Source Voltage.

**VMU** Vehicle Management Unit.

**VPW** Voltage Battery Power.

**VSI** Voltage Source Inverter.

# Chapter 1

# Introduction

## 1.1 Scope of the Thesis

The rapid evolution of electric vehicles (EVs) has brought significant advancements in automotive technology, addressing global environmental concerns and reducing reliance on fossil fuels. A central component of the efficient operation of EVs is the traction inverter, which converts direct current (DC) from the vehicle's battery into alternating current (AC) required by the electric motor. The performance and reliability of the traction inverter significantly influence the overall efficiency, power output, and driving range of the EV.

A key element within the traction inverter is the control board, which manages the precise flow of power between the battery and the motor, ensuring optimal performance across varying driving conditions. The control board implements complex algorithms to regulate motor speed, torque, and energy regeneration. It also interfaces with the vehicle's sensors and communication systems to gather essential data for real-time decision-making.

The primary motivation for this thesis is the demand for a high-performance control board capable of piloting different types of traction inverters and motors. This board shall be compliant with automotive safety standards and communication protocols, incorporate the necessary interfaces for sensor data acquisition, and host a microprocessor with adequate computational power to process data and control the inverter and its associated loads with precision.

This thesis focuses on the design of a control board, employing innovative approaches for traction inverters used in electric vehicles. Through a combination of theoretical analysis, simulation, and experimental validation, this research offers practical solutions to improve the design and implementation of traction inverter control boards. The outcome is a high-performance, versatile control board that meets the rigorous requirements of modern electric vehicles.

## 1.2 Thesis Framework

This thesis was done in Ideas & Motion S.r.l. [6] (I&M) within the frame of HiEFFICIENT European project [7]. I&M is an innovative Italian SME that provides engineering services (both HW and SW) to OEM and Tier1 companies in the automotive industry, while also being active as a supplier of Electronic Control Units (ECU) in niche applications with low volumes and high technological contents as well as developing Intellectual Property (IP) cores for integrated circuits. The company is based in Cherasco (CN)- Italy.

HiEFFICIENT stands for Highly EFFICIENT and reliable electric drive trains based on modular, intelligent, and highly integrated wide bandgap power electronics modules. The project develops high-efficiency, reliable, and compact power electronics solutions for electric and hybrid vehicles, as well as for industrial and renewable energy applications. The project aims to improve power density, system efficiency, and reliability by utilizing cutting-edge semiconductor technologies such as Silicon Carbide (SiC) and Gallium Nitride (GaN). HiEFFICIENT addresses key challenges in thermal management, power conversion, and system integration, aiming to enhance energy efficiency, lower costs, and facilitate the widespread adoption of electric mobility and green energy systems.

Within the HiEFFICIENT project, I&M is responsible for the complete design, development, and prototyping of an automotive-grade traction inverter for hybrid and electric vehicles. The company oversees the entire process, from defining technical specifications to producing a working prototype, which will then be integrated into the project's demonstrator. I&M's extensive experience in ECU design and validation is a key factor in meeting the stringent automotive safety standards and performance expectations.

## 1.3 Organization of the Thesis

This thesis is organized into several chapters, beginning with an overview of **Traction Inverters**, discussing their main components and topologies. The **Control Board** chapter highlights the main features and design tools used, followed by the **Power Supply** chapter, which covers both external and on-board power supplies. The thesis then addresses **Analog and Digital Position Sensors**, focusing on the design, simulation, and testing of their conditioning circuits. The **Programmable Inputs** chapter details the implementation of flexible input circuits, while the **Safety Features** chapter explains the design of overcurrent, overvoltage, and safety logic circuits. The **SPI Level Shifter** chapter discusses the solution adopted to manage SPI communication between 5 V and 3.3 V devices, followed by a chapter on **PCB Design**. The thesis concludes with a **Conclusions** chapter summarizing the key design choices and findings.

# Chapter 2

# Traction Inverter

Various inverter topologies have been extensively studied in the literature, each offering distinct advantages and disadvantages that make them suitable for specific applications. In the automotive industry, the voltage source inverter (VSI) is the most commonly used configuration due to its favorable efficiency-to-cost ratio. This makes the VSI particularly attractive for electric vehicle applications, where achieving a balance between performance, cost, and efficiency is critical for the overall system design.

The basic operation of a voltage source inverter involves rapidly switching the DC input on and off to create a series of pulses. These pulses are then modulated to approximate an AC waveform. Rather than directly producing a sinusoidal output, the inverter creates a pulse-width modulated (PWM) rectangular waveform, where the duty cycle is modulated in a sinusoidal manner to mimic the desired AC waveform. The duty cycle is adjusted to control both the amplitude and frequency of the fundamental component of the output voltage, ensuring that it matches the desired specifications for driving the connected AC motor.

Since the output voltage of an inverter is non-sinusoidal, it contains a high level of harmonics content. These harmonics are undesirable as they can cause motor overheating, vibration, and pulsating shaft torque [8]. High-order harmonics can be eliminated using appropriate filters, however, in automotive applications, the inductive load of the motor's stator windings is usually sufficient to filter out high-order harmonics and isolate the fundamental frequency component that drives the AC machine.

In the context of EV, the load of the traction inverter is always an electrical machine (EM). The type of machine employed in automotive traction applications varies depending on specific requirements. However, all of these machines share the capability to operate both as a motor, converting electrical energy into mechanical energy to drive the wheels, and as a generator, converting mechanical kinetic energy into electrical energy to slow down the vehicle. This dual functionality is highlighted by the term "machine" rather than simply "motor."

To effectively utilize this dual capability, the traction inverter connected to the machine must be bidirectional. This means that the power converter should act as a proper inverter when driving the motor (motoring mode) and as a rectifier during braking (braking mode) when the EM operates as a generator. The energy recovered during braking can either be dissipated through a resistor (dissipative braking) or fed back into the battery (regenerative braking), thereby extending the EV's driving range.

The classifications of inverters can be based on various criteria such as the number of phases generated on the output, the number of voltage levels, and the type of power devices used. Since most of the high-efficiency motors used in EVs operate on three-phase AC power, we will focus on three-phase traction inverters. The board designed within this thesis work is also based on three-phase voltage source inverters.

## 2.1 Main Components

A typical voltage source traction inverter consists of several key components. An overview of these components within an electric vehicle application is provided below.

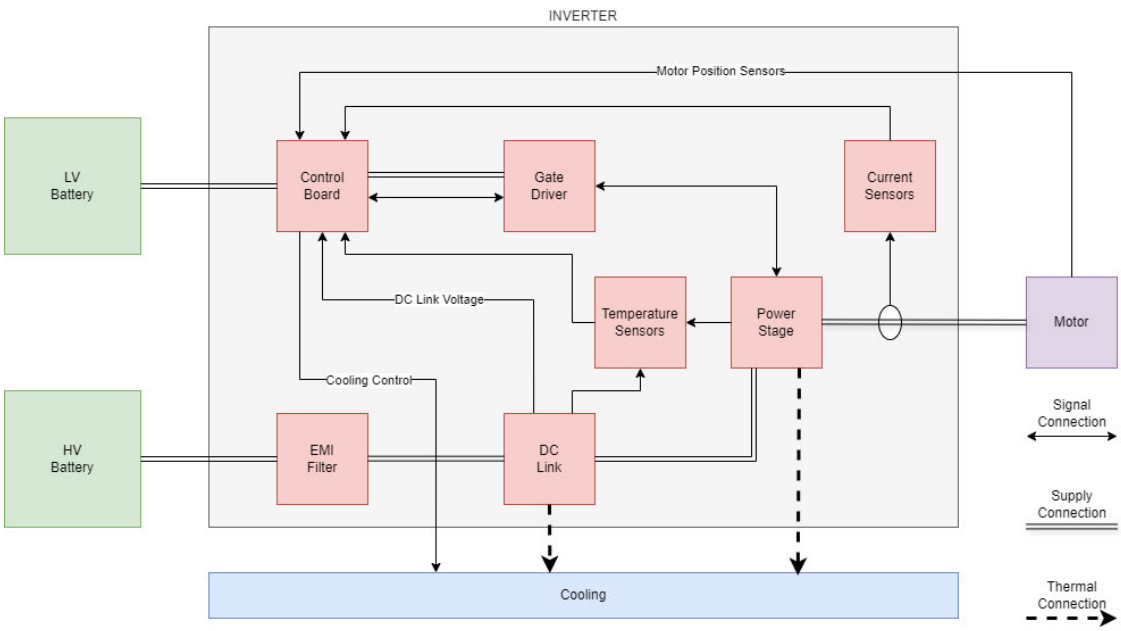


Figure 1: *Schematized view of an inverter system within an EV powertrain.*

### Power Stage

This is the core component of the inverter, where DC power from the high-voltage (HV) battery is converted into AC power to drive the motor. It comprises power electronic switches controlled by the gate drivers. The power stage handles high currents and voltages, making its efficiency and thermal management critical to the overall performance of the inverter. Traditionally, the automotive industry has relied on IGBT (Insulated Gate Bipolar Transistor) technology for this purpose. However, recent advancements in wide bandgap semiconductors have led to the adoption of SiC (Silicon Carbide) and GaN (Gallium Nitride) based power stages. These semiconductors offer significantly lower gate capacitance, enabling faster switching times. This key feature reduces switching losses and allows the power converter to operate at higher switching frequencies, which offers several advantages. Increasing the switching frequency creates a greater separation between the motor's fundamental driving frequency and the switching frequency, making it easier to filter out higher-order harmonics.

### Gate Driver

The gate driver is responsible for controlling the switching of transistors in the power stage by converting low-power control signals (typically 0-5 V) from the control board into higher voltage signals, tailored to the specific semiconductor type, to efficiently operate power electronic switches. N-type transistors are generally preferred for both high-side and low-side switches in traction inverter applications, as they offer lower conduction losses compared to P-type. However, driving the high-side N-type transistor requires specialized circuits, such as a charge pump or bootstrap capacitor, to generate a gate voltage higher than the nominal battery voltage. These circuits, along with the corresponding drivers, form the core of the gate driver board. Additionally, the gate driver provides insulation between the control board and the power stage, preventing high voltages from reaching the logic circuits thereby maintaining the safety and integrity of the system.

### Control Board

The control board's task is to manage the operation of the inverter. It receives inputs from various sensors getting information regarding phase currents, DC-Link voltage, motor position, and temperature of various components. It processes these inputs and then controls the gate driver to modulate the operation of the power stage. The onboard microcontroller can run different algorithms based on the operating condition of the whole vehicle system to optimize power conversion and manage safety functions. The control board also allows the communication of the inverter with the rest of the vehicle via CAN (Controller Area Network) or via other vehicle communication protocols. To eliminate redundancy in control

systems, modern inverter designs, such as the one developed by I&M under the HiEFFICIENT European project, incorporate a single control board capable of managing multiple inverters. This approach is particularly advantageous in electric vehicles (EVs) with multiple motors, where a unified control board can efficiently coordinate the operation of multiple traction inverters, reducing system complexity, cost, and space requirements.

### Current Sensor

The current sensors monitor the current flowing to the motor, providing essential feedback to the control board. This feedback allows the control board to regulate output power efficiently and protect the system from overcurrent conditions. Properly managing the phase shift between the current and voltage waveforms at the inverter output is crucial for optimal motor control, as the rotating magnetic field in the stator is directly influenced by the current. The current sensing circuitry can either be integrated directly into the power stage or placed on a separate board. In both cases, the sensors are positioned in close proximity to the three-phase lines and typically utilize Hall-effect technology. To ensure system safety, the sensor itself or the feedback signals must be galvanically insulated from the phase line voltages before reaching the control board. This prevents high voltages from reaching the logic circuits in the event of a fault.

### DC-Link and EMI Filter

The DC-Link is an energy storage element that acts as a buffer between the high-voltage (HV) battery and the power stage. In the voltage source inverter, its design includes capacitors that smooth out voltage fluctuations, providing a stable DC voltage to the power stage. Since the output voltage of an inverter is impulsive, the input power is also impulsive. Therefore, the buffer function of the DC-Link is crucial as it acts as a reservoir that can handle impulsive power while ensuring smooth absorption from the battery. However, even with the DC-Link, the switching action introduces a significant amount of high-frequency disturbances into the battery power line. To prevent these disturbances from affecting the battery, an electromagnetic interference (EMI) filter is placed between the DC-Link and the battery. Without this filter, such disturbances could potentially cause the battery management system to disconnect the battery.

### High Voltage Battery

The High Voltage (HV) battery provides the primary power source for the inverter and motor. It operates at a high voltage (typically several hundred volts) and supplies the energy required for propulsion. The battery pack is the most expensive part of an EV, with its cost significantly affecting the overall vehicle price

[9]. It consists of multiple cells, typically lithium-ion, which are arranged in series and parallel to form modules. These modules are integrated into the battery pack, which includes thermal management and protection systems. The Battery Management System (BMS) monitors cell voltage, current, and temperature to ensure optimal performance and longevity [10]. The standard nominal voltage for electric vehicle batteries is typically 400 V. However, the automotive industry is increasingly moving toward 800 V and higher, as this allows for significant current reduction at the same power level. This reduction translates into benefits such as thinner wiring (requiring less copper, thus less weight), reduced overheating due to the Joule effect, and other efficiency gains. However, this increase in voltage presents new challenges, particularly with the fast-charging infrastructure, which is primarily designed for 400 V systems.

### Low Voltage Battery

This battery supplies power to the low-voltage (LV) components of the inverter system, including the control electronics. In automotive applications, the standard low-voltage battery typically operates at 12 V. However, this type of battery is responsible for powering a variety of vehicle accessories such as infotainment systems and electronic actuators like windshield wipers, electric windows, or seat adjustments. Although the nominal voltage is 12 V, it generally operates closer to 13.5 V. The acceptable operating output voltage range is between 9 and 16 volts, with occasional voltage spikes reaching up to 18 V. This automotive standard is a legacy of traditional internal combustion engine vehicles, which use lead-acid batteries for auxiliary services.

### Motor

The motor is the load driven by the inverter, converting the electrical energy supplied by the inverter into mechanical energy that powers the vehicle's movement. Theoretically, a three-phase inverter can control any three-phase AC machine, though different machines require distinct control strategies and signals. For instance, to properly control an induction motor (IM), the rotational speed is a crucial feedback signal, while for a permanent magnet synchronous machine (PMSM), the rotor position is the fundamental parameter [11]. An inverter can also drive a brushless DC motor (BLDC) by generating a trapezoidal current in the phases; however, due to its high torque ripple, this type of motor is not typically used in electric vehicles. PMSMs offer numerous advantages, such as high efficiency, power factor, torque density, robustness, and reduced maintenance. The high-energy permanent magnets employed in PMSMs reduce overall motor volume and stator losses, enhancing efficiency by eliminating rotor copper losses. Despite

challenges like the cost of magnets, risk of demagnetization, and additional control requirements, the technical benefits of PMSMs have led to their widespread adoption in traction applications [12].

### Temperature Monitor and Cooling System

The temperature monitor tracks the thermal conditions of the inverter components, particularly the power stage and DC-Link. It provides critical data to the control board, enabling thermal management strategies such as reducing power or triggering cooling mechanisms to prevent overheating and ensure reliable operation. Efficient cooling is essential to maintain the performance and longevity of the inverter, as power electronic components can generate significant heat during operation. The cooling system could include liquid or air cooling, depending on the design.

## 2.2 Three Level Inverters

As previously mentioned, the Voltage Source Inverter (VSI) remains the most commonly used inverter topology in modern electric vehicles (EVs) due to its high efficiency, simplicity, and reliability. Its architecture is cost-effective and easy to manufacture, offering a significant advantage for mass-market EV production.

However, the VSI does present some limitations. The large DC-Link capacitor, necessary for stabilizing the DC voltage, can represent a substantial portion of the inverter's total volume and cost. Additionally, the requirement for a dead time between the high and low-side switches to avoid short-circuiting introduces distortion in the AC output that contributes to increased torque ripple [13][14].

Despite these downsides, the primary limitation of the VSI is that the maximum AC output voltage cannot exceed the DC bus voltage, as it is inherently a buck-type topology. This becomes a significant constraint when driving more powerful motors that require higher voltage levels. To accommodate such voltages, the power switches would need to withstand extremely high breakdown voltages, a requirement that current semiconductor technologies have not yet fully met.

For this reason, as the automotive industry moves toward higher battery voltages, such as 800 V systems, multilevel inverters have gained attention as a viable alternative to the traditional two-level VSI. The 3-phase, 3-level Neutral Point Clamped (3L-NPC) inverter is particularly promising. This topology introduces an additional output voltage level, effectively halving the voltage stress on the power switches compared to a two-level voltage source inverter. This enables the use of higher battery voltages without introducing stress-related issues to the power components. Additionally, the extra voltage level reduces total harmonic distortion (THD) in the output waveform, allowing for lower switching frequencies to achieve

the same power quality as a two-level inverter, thereby reducing switching losses [15].

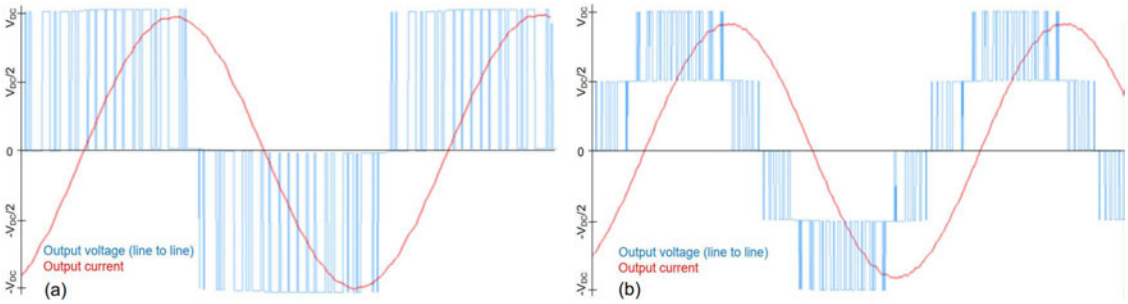


Figure 2: *Line to line voltage and current of a 2L-VSI (a) and 3L-NPC (b) [1].*

The 3-level inverter is not without its challenges. The increased number of components, such as additional transistors and diodes, increases the complexity of the control circuitry and adds to the overall cost and size of the system. Additionally, maintaining voltage balance between the different voltage levels can be challenging and often requires more sophisticated control algorithms to ensure proper operation. Despite these challenges, the 3-level inverter offers a compelling solution for high-power applications where efficiency and power quality are critical [15].

## 2.3 I&M Voltage Source Inverter

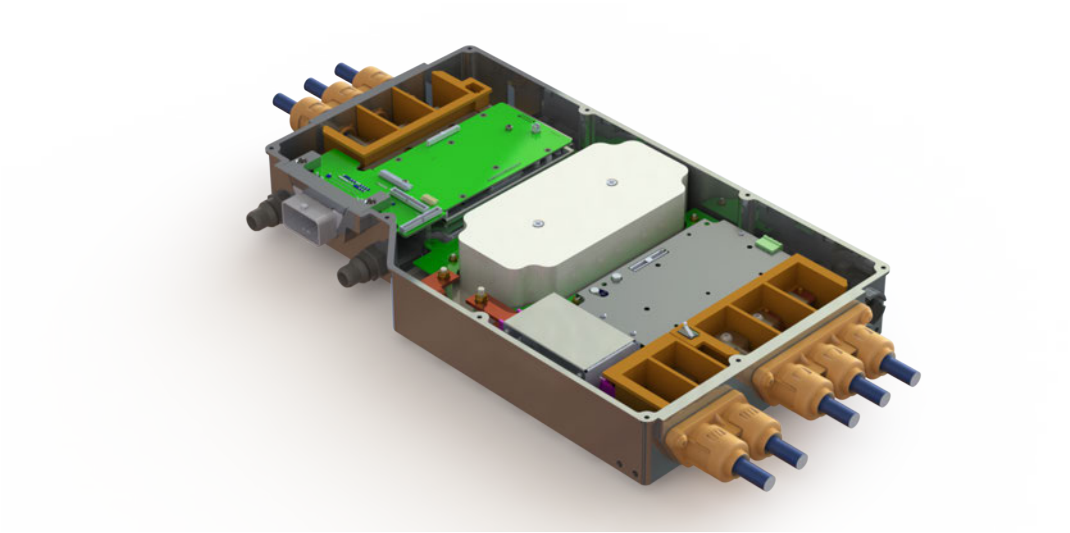

Figure 3: *Complete inverter design showing the dual voltage source implementation.*

The traction inverter design developed by I&M, as shown in Fig. 3, is based on a dual voltage source inverter configuration. Central to the design is the DC-Link,

which is located in the middle of the inverter and surrounded, on both sides, by the power, driver, and control board layers, all organized in a compact and efficient sandwich structure.

The control board, designed in this thesis, is capable of managing both inverters, allowing for a single control board to drive the entire system. A dedicated connector links the control board to the gate driver beneath it, while the second inverter is connected via a flat cable that passes over the DC-Link, ensuring seamless integration with the second gate driver and power module. This efficient setup reduces the need for additional control hardware, streamlining the overall system design.

The three-phase voltage lines exit the inverter enclosure on both sides, while the high-voltage battery connection is positioned at one end. Internally, the battery line passes through an EMI filter before reaching the DC-Link via bus bars, ensuring stable and noise-free power delivery. For thermal management of the DC-Link, a thermal coupling pad is positioned beneath it, enhancing heat dissipation through the enclosure.

Moreover, the inverter external connector provides low-voltage power to the control board, along with communication lines and feedback signals from sensors such as position sensors. Adjacent to this connector are the liquid cooling inlet and outlet ports, which are designed to interface with an external cooling system. The cooling system, potentially controlled by the inverter's control board, ensures thermal stability and reliable performance under varying load conditions.

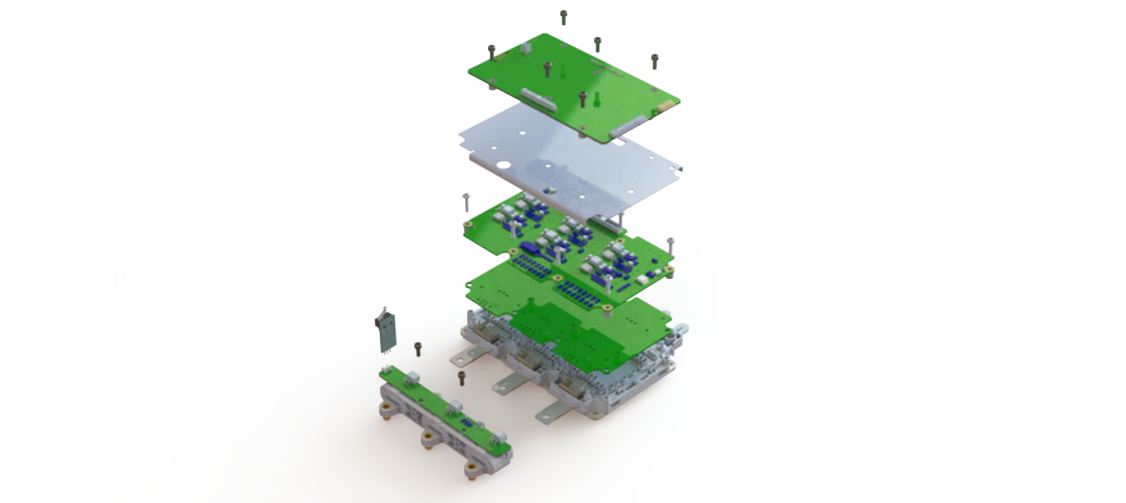

Figure 4: *Exploded view of the inverter design showing control, driver, and power boards, including current sensing PCB.*

To ensure safety, the cap of the inverter enclosure is designed with two windows for proper connection of high-voltage cables. When closed, these access points press

down a switch that ensures continuity in the high-voltage interlock loop (HVIL), preventing high voltages from being present when the enclosure is open.

An exploded view of the layered architecture of power, driver, and control board, is displayed in Fig. 4 where the current sensing circuit is implemented on a dedicated printed circuit board (PCB) near the three-phase output lines for precise current measurement.

The current sensing PCB is based on Hall effect sensors supplied by LEM, which are known for providing accurate and reliable current measurements. LEM's current sensors feature galvanic isolation, ensuring the separation of the measurement system from the primary circuit for safety and precision. These sensors, which include protection mechanisms and low-offset characteristics, are particularly suited for applications in electric vehicles, motor control, and battery management systems [16].

The power stage is based on the Infineon HybridPACK™ Drive form factor, a compact power module tailored for electric and hybrid vehicle traction inverters. Its advantages include high power density, optimized efficiency, soft switching behavior, and the integration of advanced silicon IGBT or SiC MOSFET technologies [17]. Efficient thermal management is achieved as the fins of the power module are in direct contact with the liquid in the cooling circuit, located at the bottom of the inverter enclosure.

The power module is connected to the driver board through a "routing" board, which handles measurements and safety features, such as high-voltage isolation. The control board is mounted on top of the driver board, shielded by a protective cover that ensures electromagnetic interference immunity between the control and driver boards.

In parallel with the dual voltage source inverter, a single inverter solution has also been developed. In this design, the inverter section near the connector is removed, and the connector is relocated closer to the bus bars, between the DC-Link and the EMI filter, resulting in a more compact layout. A figure of this enclosure is presented in Fig. 5.

Figure 5: *Enclosure of the single inverter design.*

# Chapter 3

# Control Board

## 3.1 Main Features

This section presents the key design elements and operational features of the control board developed in this thesis.

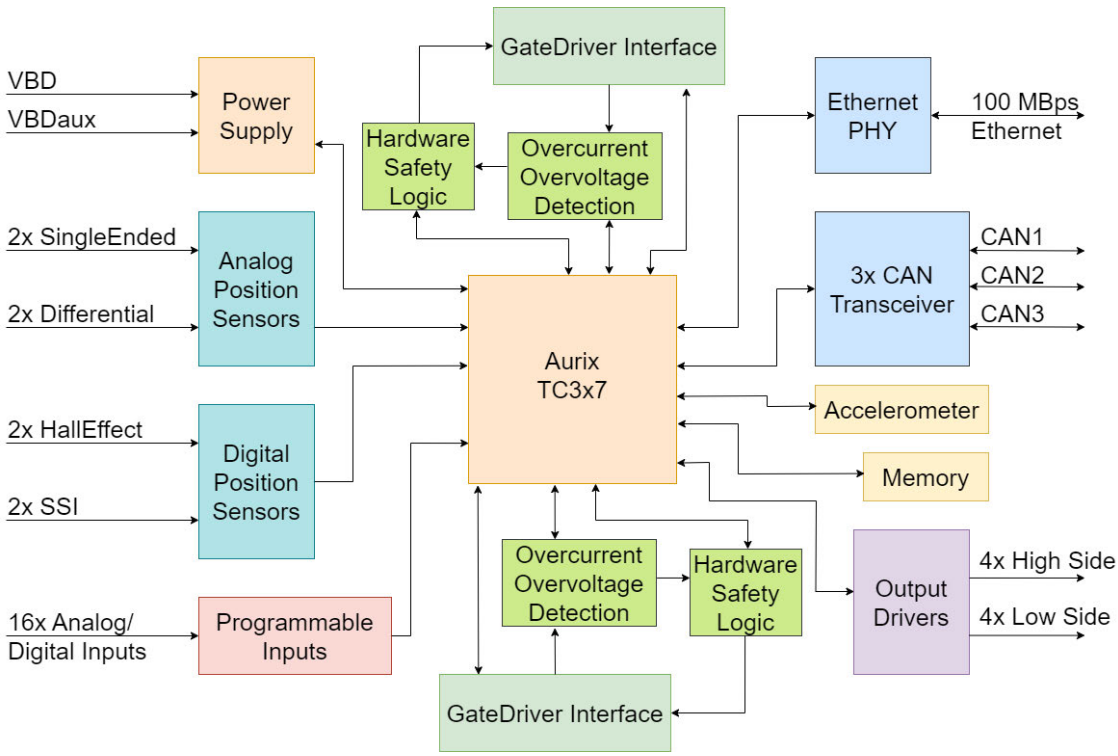


Figure 6: *Overview of the control board architecture*

### Microcontroller

The Microcontroller Unit (MCU) is the core component of the control board, designed to meet the specific requirements of electric powertrain applications in terms of performance, standard compliance, voltage levels, and functional integration. The board utilizes an Infineon AURIX™ TriCore™ TC3x7 microcontroller, aligning with I&M reference design for software development.

The AURIX™ family of microcontrollers is built around the TriCore™ cores. The TriCore™ is a unified 32-bit microcontroller DSP architecture, optimized for real-time embedded systems. Its Instruction Set Architecture (ISA) combines the real-time capabilities of a microcontroller, the computational power of a DSP, and the performance efficiency of a RISC load/store architecture, all within a compact, re-programmable core. The AURIX™ MCU chosen for this project offers a multi-core architecture, advanced security, functional safety (ASIL-D compliance), and connectivity features. Additionally, it integrates with the Multi-Voltage Safety Microprocessor Supply (TLF35584) [18].

### Power Supply

The control board is designed to be powered at 12 V nominal and includes a power management integrated circuit (PMIC), the TLF35584, that generates the main onboard voltages required by the system.

The TLF35584 is a multi-output system supply designed for safety-critical applications, providing efficient and flexible power regulation for microcontrollers, transceivers, and sensors over a wide input voltage range. It supports 5 V or 3.3 V outputs for MCUs and includes various safety features such as UV/OV monitoring, flexible watchdogs, error monitoring, and a safe state controller, which are crucial for achieving ASIL-D compliance. The device is ideal for use in automotive systems like electric powertrains, braking, and chassis controllers, well integrated with Infineon's AURIX™ microcontrollers [19].

### PWM Control Signals

The board is capable of generating 18 PWM signals with precise control over blanking times, making it suitable for driving one or two Voltage Source Inverters (VSIs). Additionally, this feature enables the control of a three-level ANPC inverter, which requires 6 PWM signals per leg, offering enhanced flexibility for various powertrain configurations. The precise control of blanking times is made possible by the Generic Timer Module (GTM) architecture integrated into the AURIX™ TriCore™ MCU. The GTM manages complex timing functions in embedded systems, particularly in automotive applications, through its specialized sub-modules for PWM generation, signal processing, motor control, and safety features. By offloading timing-related tasks from the CPU, the GTM reduces system interrupts, while its

scalable architecture and integration with peripherals like ADCs make it highly configurable for diverse applications.

### Communication Interfaces

The control board is equipped with advanced communication capabilities, featuring three CAN transceivers and a Ethernet (100BASE-TX) interface. These interfaces provide robust, high-speed communication with the vehicle's central management unit (VMU) and other subsystems, ensuring reliable data exchange for control operations and system diagnostics. One of the CAN transceivers includes a wake-up option, which allows the turn-on of the control board via CAN, without the need for the key signal. The Ethernet interface is particularly useful for tasks such as real-time debugging and detailed diagnostics. Additionally, the CAN interface allows for firmware updates to the control board, enabling VMU over-the-air (OTA) software updates to be flashed to the control board without requiring a manual update at an authorized service center. The CAN physical layer can also be utilized for UART communications, as the microcontroller pins responsible for managing CAN can be reconfigured to function as UARTs. This design flexibility allows for maximum adaptability, enabling the control board to support various communication protocols as needed.

### Sensor Inputs

The control board is mainly designed for the dual voltage source inverter, meaning that it must be able to receive position feedback from two motors. To enhance the board's adaptability to different motor and sensor configurations, conditioning circuits for both digital and analog position signals are provided for each motor, offering flexibility in sensor integration. Additionally, the board includes 2 SSI (Synchronous Serial Interface) and 4 SENT (Single Edge Nibble Transmission) interfaces, which allow it to receive precise information from various sensors.

The board also includes an onboard accelerometer, adding the ability to monitor and respond to vehicle dynamics, further enhancing control precision and contributing to the overall stability and performance of the vehicle.

### I/O Capabilities

The board includes a range of general-purpose analog and digital inputs, enabling it to interface with various sensors and control signals within the vehicle. These inputs can be programmed via software according to the application's requirements, allowing for customization to suit incoming signals. Configurable features include a low-pass filter with an adjustable cutoff frequency and selectable pull-up or pull-down resistors, available in either strong (some k$\Omega$) or weak (tens of k$\Omega$) configurations.

The control board includes 4 low-side and 4 high-side outputs, offering versatile control options for managing auxiliary systems and driving various actuators within the vehicle. These outputs enhance the board's capability to control auxiliary functions, such as low-power modules and vehicle actuators, across a range of applications.

#### Safety Features

The board incorporates a hardware protection circuit designed to detect motor phase overcurrents, DC-Link overvoltage, and manage inverter safe states through dedicated safety logic. Overcurrent protection is essential for preventing motor damage and ensuring system safety, as excessive current can lead to overheating and, in severe cases, component failure. By employing hardware-based detection for rapid response, the system minimizes hazardous conditions, extends equipment lifespan, and maintains safe operation.

Equally important is the monitoring of DC-Link overvoltages to safeguard both the inverter and the connected components. Overvoltages can lead to insulation breakdown, excessive heat, and potential damage to the battery.

The board also includes hardware safety logic for interfacing with gate drivers, capable of managing two safe state signals to support four possible safe states. This hardware-based safety logic operates independently of the microcontroller, ensuring it can still respond in the event of a microcontroller failure, thereby enhancing the overall safety and reliability of the system.

#### Memory

The board is equipped with 1 MB of F-RAM, offering non-volatile, high-speed memory for storing critical data. This memory serves as a black box in the event of an inverter system failure. Essential operational parameters are periodically written to the memory, enabling the reconstruction of failure events. By capturing data such as phase voltages and currents, DC-Link voltage, and switching state, it provides crucial insights for failure analysis.

## 3.2 Design and Testing Tools

The circuit designs developed during this thesis and integrated into the control board were carried out using Siemens Xpedition Enterprise [20], a widely used industry-standard software for PCB development.

During the schematic design process, microcontroller pin assignments were facilitated by Infineon's AURIX™ Development Studio [21], which allows users to select a specific Infineon microcontroller and assign, through its pin mapper, the appropriate pins for desired functions.

During the evaluation of power losses, MATLAB, a programming and numerical computing platform developed by MathWorks [22], was used to perform complex calculations and generate graphs for visual analysis.

Simulations of each design were performed using LTspice, a simulator developed by Analog Devices [23], which enables users to probe schematics and analyze results through its built-in waveform viewer.

Lastly, tests were conducted on real components to validate the simulation results under real-world conditions. The instruments used during testing included a multimeter, bench power supply, signal generator, oscilloscope, and Analog Discovery 2. A detailed list of the instruments used can be found in Table 7.

| **Device** | **Brand** | **Model** | **Serial Number** |
|---|---|---|---|
| Multimeter | Fluke | 175 - True RMS | 50250491 |
| Multimeter | Fluke | 179 - True RMS | 58590413 |
| Power Supply | TTI | EX354RD - 280W | 366245 |
| Power Supply | TTI | CPX400DP - 420W | 387492 |
| Signal Generator | GW Instek | MFG-2260MFA | GET852262 |
| Oscilloscope | Teledyne Lecroy | HDO9104, 40GSa/s | LCRY4404N30209 |
| Oscilloscope | Rohde Schwarz | RTO 1014,10GSa/s | 1316.k14-400035 |
| USB Oscilloscope | Digilent | Analog Discovery 2 | 210-321 |

Figure 7: *Table with test equipment used.*

# Chapter 4

# Power Supply

The low-voltage power supply architecture of the traction inverter system is designed to ensure robust and reliable operation under varying conditions, including protection against reverse polarity and redundancy in power sources. This chapter describes the key components and pathways involved in delivering power to the control board.

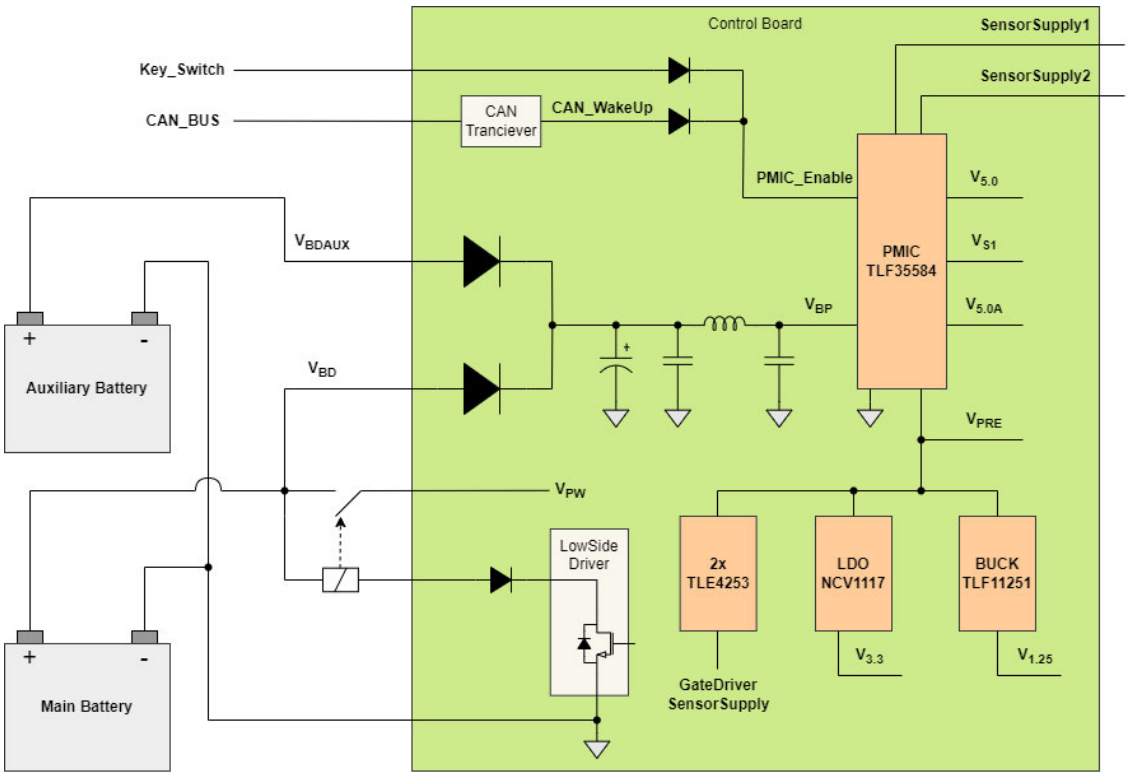


Figure 8: *Power Supply Scheme of the Control Board.*

## 4.1 External Supply

### VBD (Battery Direct)

The primary power input to the board is derived from the Main Battery with a nominal voltage of 12 V, typically ranging between 9 and 16 volts. The direct connection from the Main Battery is designated as VBD (Battery Direct). To safeguard the control board against the possibility of reverse polarity, the VBD line is routed through a diode. This diode protects the system from potential damage caused by incorrect battery connections.

### VPW (Battery Power)

The VPW (Battery Power) line is another crucial power path originating from the Main Battery. Unlike VBD, VPW is specifically intended to power high-side drivers, which are components within the system that may require significant current to operate.

Due to the potentially high current demands on the VPW line, employing a simple diode for reverse polarity protection would not be appropriate. A diode capable of handling high currents would generate significant power dissipation, leading to inefficiencies and possible thermal management issues. Instead, reverse polarity protection on the VPW line is achieved using an external relay.

The relay acts as a switch that physically opens or closes the VPW line. The relay remains open by default, thereby preventing any power from being present on the VPW line. Once the board is powered on (which means that the main battery is correctly connected), a low-side switch energizes the relay, causing it to close and allowing current to flow through the VPW line. This approach ensures that the VPW is protected from reverse polarity without the drawbacks of a high-current diode.

### VBDaux (Auxiliary Battery)

In addition to the Main Battery, the control board is equipped to receive power from a secondary Auxiliary Battery. The auxiliary battery is also rated at 12 V and is connected to the board through another reverse polarity protection diode as found in the VBD line. The output from the Auxiliary Battery is referred to as VBDaux.

The VBDaux and VBD lines are merged together after their respective protection diodes. This configuration effectively creates a logical OR function between the two batteries. The diodes ensure that power from each battery can flow to the board, but not back into the other battery, thereby preventing any possible cross-discharge between the two sources.

This setup provides an important redundancy: if one of the power sources fails, whether it be the Main Battery or the Auxiliary Battery, the other can seamlessly continue to supply power to the control board. This redundancy enhances the reliability of the system, ensuring continuous operation even in the event of a power source failure.

### Π Filter and VBP

Once the VBD and VBDaux lines are merged, the resulting line is filtered through a Π (pi) filter before being renamed VBP (Battery Protected) and distributed to the board's circuitry. The Π filter is composed of two capacitors connected by an inductor, arranged in a configuration that resembles the Greek letter Π. Serving primarily as a low-pass filter, it effectively blocks high-frequency noise and electromagnetic interference (EMI). The design of the Π filter ensures that it attenuates noise in both directions: protecting the board from power supply noise and preventing EMI from being injected back toward the battery line. Furthermore, the Π filter plays a crucial role in ripple attenuation, ensuring that the board's components receive a smoother DC voltage.

### Key Switch and CAN Wake-Up Signals

The board's power-up sequence can be initiated by two control signals: the Key Switch signal and the CAN Wake-Up signal. The Key Switch is typically connected to the vehicle's ignition system, providing a signal when the ignition is turned on. The CAN Wake-Up signal, on the other hand, originates from the vehicle's CAN bus and is used to wake the system up from a low-power state. Either of these signals can independently power on the board depending on which one occurs first.

This is accomplished by combining the two signals using a diode OR configuration. Each signal is directed through its respective diode before being merged into a single line. This combined signal then serves as the input to the PMIC Enable Pin on the board. When either of the two signals becomes active, the Power Supply Enable Pin is triggered, initiating the power-up sequence and activating the board's operation.

## 4.2 On-Board PMIC

The board's power management system is based on the Infineon TLF35584, a multi-output system IC designed for safety-critical applications. This IC provides a stable 5 V supply to components such as the microcontroller, transceivers, and sensors. Its efficient operation across a wide input voltage range is made possible by an advanced pre- and post-regulator architecture, which ensures reliable performance even under varying power conditions. This IC incorporates multiple safety features

that facilitate an ASIL-D compliant design when paired with Infineon's AURIX™ MCUs. This compliance is crucial for applications demanding the highest levels of functional safety, such as in automotive systems.

The TLF35584 provides seven different voltage outputs, each tailored for specific requirements within the system:

| **Outputs** | **Nominal Voltage (V)** | **MAX Current (mA)** | **Comments** |
|---|---|---|---|
| Vpre | 5.8 | 1500 | Buck generated, high ripple |
| V5.0 | 5 | 600 | LDO generated, for microcontroller supply |
| VS1 | 5 | 200 | LDO generated, for peripherals supply |
| V5.0A | 5 | 150 | LDO generated, for ADC and voltage references, highly stable |
| VSS1 | 5 | 150 | V5.0A tracking, for sensor supply |
| VSS2 | 5 | 150 | V5.0A tracking, for sensor supply |
| Vstb | 5 | 10 | Standby supply (not used) |

Figure 9: *Table of outputs with nominal voltage, max current, and comments.*

Here is a detailed output analysis:

- **Vpre**: This 5.8 V output, sourced from the switching pre-regulator converter within the IC, is capable of delivering up to 1500 mA. It exhibits significant ripple, which may necessitate additional filtering depending on the application sensitivity.

- **V5.0**: Reserved exclusively for the microcontroller, this 5 V output is generated by an internal LDO regulator, providing stable and clean power essential for MCU operations.

- **VS1**: Also a 5 V output, VS1 is designed to power communication protocols and other peripherals with a modest current limit of 200 mA.

- **V5.0A**: Another 5 V output, known for its exceptional stability and low noise. This line is ideal for analog voltage references and ADC conversions, ensuring precise and reliable readings.

- **VSS1 and VSS2**: These 5 V outputs are designed to supply external sensors, tracking the stability and cleanliness of V5.0A.

In addition to the sensor supply outputs generated by the TLF35584, which provide power to motor position sensors off the board, two additional voltage trackers have been implemented to power other sensors (including current sensors) via the

gate-driver interface. These voltage trackers are sourced from Vpre and configured to track the V5.0A output, ensuring stable and consistent voltage delivery. The TLE4253E IC was selected for this purpose to ensure that both the sensors and the ADC share the same reference voltage, thereby improving the accuracy and reliability of sensor readings.

In addition to the Infineon TLF35584 PMIC, which powers the 5 V circuits, the board employs two specific DC-DC converters to further regulate the power supply to lower voltage levels:

- **3.3 V:** The 3.3 V required for powering some of the board's logic circuits, such as the Ethernet interface, and other components is generated by an LDO (Low Dropout Regulator), specifically the NCV1117ST. This LDO steps down the 5.8 V output from Vpre to 3.3 V. Favored in applications where noise sensitivity is a concern and the input-to-output differential is minimal, LDOs help maintain a clean and stable output voltage with minimal power loss.

- **1.25 V:** The generation of 1.25 V is handled by a buck converter, the TLF11251LD, which efficiently reduces Vpre's 5.8 V down to 1.25 V. This voltage is crucial for powering internal functions of the microcontroller, such as its core logic. The lower voltage significantly reduces the overall power consumption of the microcontroller, which is essential for minimizing heat generation and enhancing energy efficiency. Buck converters are preferred when there is a substantial difference between the input and desired output voltages, offering better efficiency than LDOs under such conditions and thereby minimizing heat production.

## 4.3 Power Consumption Estimation

During the control board design, it is essential to verify whether the onboard Power Management IC (PMIC) can supply the required current. This is crucial to prevent power failure of on-board circuits or overheating, which could lead to malfunction or damage to the board.

The current consumption for each board component was estimated based on datasheet specifications. In addition to the primary components, design choices such as pull-up resistors, especially those with low resistance values, were also considered, as they can draw a non-negligible amount of current, contributing to the overall power consumption during operation.

The data was organized in a spreadsheet, with the results shown in appendix A. This analysis accounts for the power consumption of all voltage regulators on the board. However, the TLF35584 was identified as the most critical component due to its configuration, which includes a switching pre-regulator and multiple Low-Dropout (LDO) post-regulators. Additionally, all other regulators draw their

current from the pre-regulator (Vpre), meaning their power consumption is indirectly sourced from the TLF35584. To accurately estimate power losses within this chip and assess its thermal performance during operation, the following approach was applied.

For each LDO output of the TLF35584, power dissipation was calculated by multiplying the drawn current for the voltage drop across the LDO. The drop is given by $V_{pre} = 5.8$ V minus $V_{out} = 5$ V, resulting in a 0.8 V difference for all the post regulators. The total power dissipation for the post-regulators on the chip was then obtained by summing the losses of each LDO. To account for the worst-case scenario, the two sensor supply outputs of the TLF35584 were estimated at their maximum rated current.

To estimate the losses in the switching pre-regulator under worst-case conditions, parameters from the TLF35584 datasheet were applied. Although it operates as a synchronous buck converter, only the two switching transistors are integrated on-chip, while components such as the inductor and output capacitors are external. Therefore, the loss estimation focuses on the switching and conduction losses of the internal transistors. The mathematical derivation presented below does not account for dead times between the two switches. However, to introduce a safety margin and compensate for this exclusion, the total current drawn from Vpre was approximated by rounding up. This leads to a higher current value, resulting in an overestimation of the losses.

### 4.3.1 Derivation of Pre-Regulator Total Power Losses

To start the following parameters are defined:

$$V_o = 5.8 \text{ V},\ I_o = 1.2 \text{ A},\ L = 22 \times 10^{-6} \text{ H},\ f_s = 400 \text{ kHz}$$
$$R_1 = 0.63\ \Omega,\ R_2 = 0.3\ \Omega,\ t_r = 14 \text{ ns},\ t_f = 18 \text{ ns}$$

The duty cycle $D$ is defined as:

$$D = \frac{V_o}{V_{\text{in}}}$$

The inductor current ripple $I_r$ is given by:

$$I_r = \frac{(V_{\text{in}} - V_o)}{L} \cdot \frac{D}{f_s} = \frac{V_o}{L} \cdot \frac{1-D}{f_s} = \frac{V_o}{L} \cdot \frac{V_{\text{in}} - V_o}{V_{\text{in}} f_s}$$

The maximum and minimum inductor currents are:

$$I_{\max} = I_o + \frac{I_r}{2}$$
$$I_{\min} = I_o - \frac{I_r}{2}$$

The RMS currents for each switch using Flat-Top Approximation are given by:

$$I_{1,\text{rms}} = I_o \cdot \sqrt{D}$$

$$I_{2,\text{rms}} = I_o \cdot \sqrt{1 - D}$$

The conduction power losses for each switch are given by:

$$P_{c1} = I_{1,\text{rms}}^2 \cdot R_1$$

$$P_{c2} = I_{2,\text{rms}}^2 \cdot R_2$$

The switching losses are given by:

$$P_{s1} = \frac{f_s}{2} \cdot (t_r \cdot V_{\text{in}} \cdot I_{\text{min}} + t_f \cdot V_{\text{in}} \cdot I_{\text{max}})$$

$$P_{s2} = \frac{f_s}{2} \cdot (t_r \cdot V_{\text{in}} \cdot I_{\text{max}} + t_f \cdot V_{\text{in}} \cdot I_{\text{min}})$$

The total power loss $P_{\text{tot}}$ is the sum of the conduction and switching losses:

$$P_{\text{tot}} = P_{c1} + P_{c2} + P_{s1} + P_{s2}$$

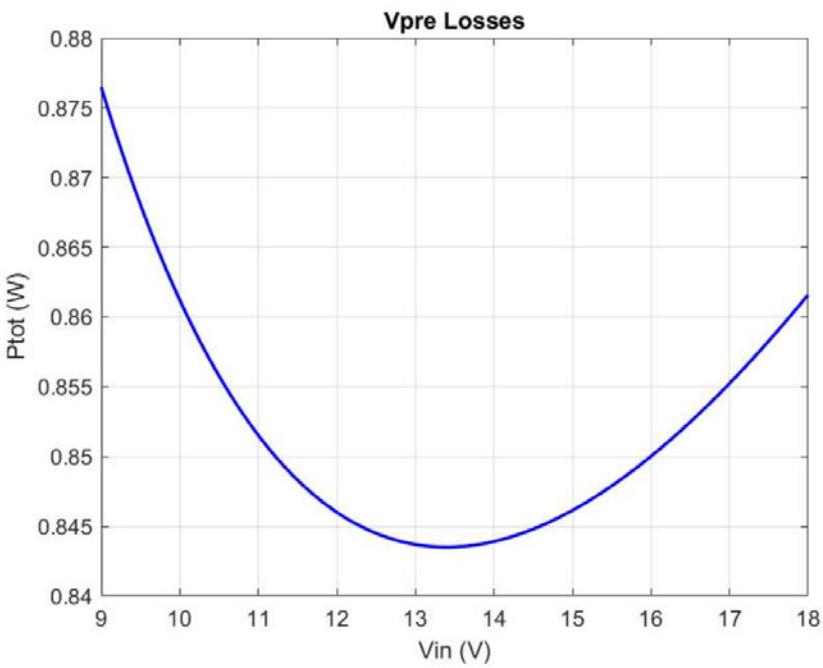


Figure 10: *Plot of the total power losses of the TLF35584 pre-regulator.*

### 4.3.2 Thermal Considerations

This mathematical derivation was then implemented in Matlab environment to obtain a plot of $P_{tot}$ vs $V_{in}$.

From Figure 10, it is evident that the total power losses ($P_{tot}$) of the pre-regulator reach their minimum near the nominal input voltage. However, as the input voltage moves towards the extremes of the operating range, the losses increase. The worst-case scenario occurs at the minimum input voltage (Vin = 9 V), resulting in a total power loss of 0.8765 W.

This value, combined with the losses from the post-regulators within the chip, leads to a total power dissipation of 1336 mW. This value is then multiplied by the thermal resistance "junction to ambient" (37 K/W), as specified in the datasheet, to calculate the temperature rise during operation. The result of this analysis shows an approximate temperature increase of 50 °C under worst-case conditions.

Considering a water cooling system temperature of approximately 60-65 °C for the inverter and a delta of 20 °C for the air inside the inverter enclosure, the operating temperature for the control board is assumed to be around 85 °C. Given this starting condition, the worst-case scenario of a 50 °C temperature rise still remains below the maximum rated temperature of 150 °C, ensuring that even under extreme load conditions, the TLF35584 remains within a safe operating temperature range.

# Chapter 5

# Analog Position Sensors

## 5.1 Overview

The control of three-phase electric machines in electric powertrains relies heavily on the accurate acquisition of rotor position. This information is essential for the proper generation of the stator magnetic field. This requirement is not limited to Permanent Magnet Synchronous Motors (PMSMs) but is also crucial for other electric machines proposed for electric powertrains, such as Induction Motors and Switched Reluctance Motors (SRM) [24].

Errors in sensor data can result in imprecise motor control, leading to various problems within the powertrain system, such as reduced efficiency, shorter driving range, and diminished driving quality due to torque ripple. These inaccuracies can be caused by several factors, including sensor misalignment, shocks, vibrations, temperature fluctuations, and magnetic interference. Additionally, data processing errors, such as latency, jitter, noise, incorrect sampling frequencies, and quantization failures, can further exacerbate these issues [25].

Traditional mechanical position sensors are commonly used to gather rotor position information. However, these sensors can introduce challenges, including increased motor volume, shaft rotation inertia, and reduced power density. The installation of these sensors increases motor complexity, raises system costs, and complicates maintenance, particularly in motors with a high pole count, where installation accuracy is crucial. [26].

To address the limitations of mechanical sensors, sensorless control technologies have been developed and have gained significant attention in motor control research. These technologies replace conventional mechanical sensors with software-based solutions that analyze motor voltage and current in real time to determine rotor position. This approach enhances detection reliability, extends motor service life, simplifies connections between inverters and motors, reduces system costs, and improves overall system reliability [26].

Despite the potential of sensorless technologies, the sensored solution offers several advantages. It enables motor operation at low speeds, where sensorless schemes fail due to insufficient back-EMF for rotor position detection, making it ideal for applications requiring maximum torque at zero speed [26]. It also ensures accurate commutation at very high speeds, where back-EMF transitions become difficult to differentiate. Additionally, sensored systems require simpler software implementation, as they eliminate the need for complex algorithms and real-time estimations found in sensorless designs. This results in reduced CPU resource usage and lower computational power requirements [27]. For these reasons and due to the automotive stringent reliability requirements the sensored rotor angle detection remains the industry standard for automotive applications [24].

A variety of rotor shaft position sensor technologies are available for PMSMs, including resolver types, inductive/eddy current-based sensors, magnetoresistive sensors, and encoders [11].

From the perspective of the control board, sensors can be categorized according to their output data into analog or digital. This chapter focuses specifically on analyzing the characteristics and integration of analog sensors, discussing how their signals are conditioned and processed within the board.

The primary challenge when interfacing external analog signals lies in ensuring that the signals fall within the acceptable input voltage range of the onboard ADC. Additionally, the conditioning circuit must be designed to effectively filter out any noise that may accumulate along the connection wiring, which is often long and exposed to environments with high electromagnetic interference (EMI).

The analog position sensors, commonly referred to as SinCos sensors, generate two analog signals in the form of sine and cosine waveforms as the motor rotates. Once these signals are digitized by the Analog-to-Digital Converter (ADC), the microcontroller calculates their ratio, representing the tangent of the angle $\theta$. To determine the angle $\theta$, the microcontroller typically utilizes a precomputed lookup table (LUT), which relates signal ratios to their corresponding angle values. To optimize size and processing speed, the LUT typically covers a limited range (e.g., 0° to 45°). Trigonometric identities are then applied to extend the calculation to the full 360° range, ensuring efficient angle computation without encountering singularities [28][29].

Depending on the sensor configuration, the connection to the control board can be either single-ended or differential. In both cases, the sensors are powered by the board via dedicated 5 V supply lines. This ensures that both the sensors and the ADC share the same reference voltage, which helps to guarantee that the sensor outputs are already within the input voltage range of the ADC.

In a single-ended connection, each signal (sine or cosine) is transmitted over a single wire, with the waveform modulated between 0 and 5 volts, meaning it includes a DC component centered around 2.5 V (half the ADC's dynamic range). This type of connection requires fewer wires and a simpler conditioning circuit, as the board

only needs to implement a low-pass filter to cancel out high-frequency noise without the need to rescale or adjust the signal for the ADC input. However, the major drawback of this configuration is its poor noise immunity, making it less suitable for noisy EMI environments, such as those found in automotive applications.

To improve noise rejection, a differential connection is often used. In this setup, each signal (sine and cosine) is transmitted over two wires: one wire carries the original signal, as in the single-ended connection, while the other transmits an inverted copy of the signal (mirrored around half dynamics: 2.5 V).

## 5.2 Conditioning Circuit Design

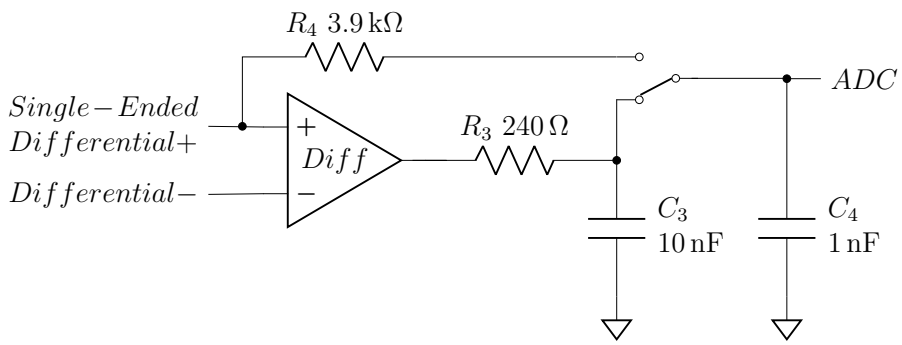


Figure 11: *Circuit diagram showing the adopted solution for conditioning single-ended and differential analog position sensor signals.*

To maintain flexibility in the board design, allowing it to accommodate both single-ended and differential input configurations, a blended solution was implemented. The single-ended input is in common with the positive input of the differential circuit, and the output selection between the two configurations is managed via an analog multiplexer.

The single-ended conditioning circuit consists of a passive low-pass RC filter, made by $R_4$ and $C_4$ chosen respectively equal to 3.9 kΩ and a 1 nF. In particular, the capacitor $C_4$ is placed after the multiplexer, close to the ADC pin of the microcontroller, to stabilize the signal and ensure consistent readings. This placement also has implications in the design of the differential circuit, as the capacitor is located on the shared line after the multiplexer, affecting both input configurations. The implemented design achieves a cutoff frequency of approximately 40 kHz. A more detailed analysis of the filtering requirements for the conditioning circuit will be discussed in the section addressing the differential analog position sensors.

To ensure compatibility with differential SinCos sensors, the onboard conditioning circuit must perform three operations: first, the signals need to be subtracted from each other; second, the result of this subtraction must be scaled down by half

to match with the ADC's input voltage dynamic; third, it must add a DC offset to translate the output signal between 0 and 5 volts. This differential configuration offers superior noise immunity because external noise affects both wires equally. By subtracting the signals, the common noise is canceled out, providing cleaner data for the control board to process.

The design solution selected to meet these requirements is an operational amplifier (op-amp) configured as a generalized adder. Another viable option considered is an instrumentation amplifier, which would provide superior common-mode noise rejection. However, this approach presents challenges in sourcing an automotive-compliant, single-supply, and compact integrated circuit at a reasonable price. Furthermore, given that the board is designed to interface with two motors, each conditioning circuit is instantiated twice, effectively doubling the cost. This made the selected design even more advantageous in terms of overall cost and component sourcing.

Two 100 kΩ pull-down resistors have been added to the differential inputs (one for each) to bring the line to GND if not used or disconnected. Given their relatively high resistance, they do not affect the operation of the generalized adder, as will be discussed and confirmed through simulation later in this chapter.

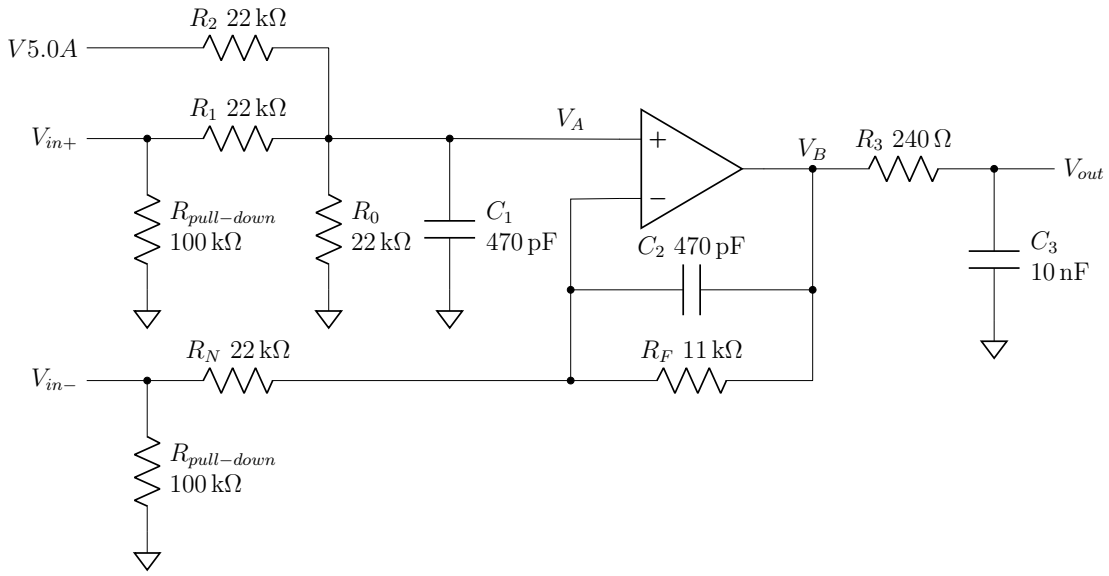


Figure 12: *Circuit diagram showing the adopted solution for conditioning the SinCos differential input signals.*

The circuit shown in Fig. 12 is designed to perform the signal conditioning functions previously described. The simple subtraction of the two input signals (which are one the inverse of the other), results in a doubled amplitude with no DC component. This would exceed the dynamic output range of the operational amplifier leading to a clamped output waveform without the negative half period.

To avoid this, the input signals are fed into the adder through two branches, each with a gain magnitude of $\frac{1}{2}$, one positive and one negative, since they need to be subtracted. This ensures that the resulting signal remains within the op-amp's operational range.

Furthermore, an offset is required to keep the output waveform within the ADC admissible range. This is accomplished through an additional branch on the positive side of the adder, which derives the necessary offset from a 5 V supply with a gain of $\frac{1}{2}$. The chosen reference voltage supply "V5.0A" is the one provided by the onboard PMIC with the lowest ripple and most stable output, to ensure a precise offset of the output waveform.

Additionally, to ensure the correct operation of the generalized adder, the following condition between branch gains must be satisfied:

$$A_p = A_n + 1$$

where $A_p$ represents the sum of all positive branch gains, and $A_n$ represents the sum of all negative branch gains. Currently, this condition is not met, as we have discussed a gain of $\frac{1}{2}$ on the negative side and two gains of $\frac{1}{2}$ on the positive side.

To balance the system, a "dummy" branch is added on the positive side with the remaining gain of $\frac{1}{2}$. This branch is connected to 0 V (GND) to ensure that the overall gain condition is fulfilled but the desired behavior on the output is not altered.

Let consider $V_{in+}$ and $V_{in-}$ represent the two input signals, and let $V_B$ represent the output of the adder. The overall desired transfer function of the circuit is described by the following equation:

$$V_B = \frac{1}{2}V_{in+} - \frac{1}{2}V_{in-} + \frac{1}{2}\text{V5.0A} + \frac{1}{2}\text{GND}$$

The resistors in the circuit define the gain for each branch. Let $R_{in}$ represent a generic input resistor in a generic input branch, and $R_f$ represent the feedback resistor. Since the gain is uniform across all branches, in this particular case, the following relationship holds:

$$\frac{R_f}{R_{in}} = \frac{1}{2}$$

This result indicates that identical input resistors are used for each branch, meaning $R_{in} = R_N = R_0 = R_1 = R_2$. In the final implementation, 22 kΩ resistors were used consistently throughout. To meet the requirement for the feedback resistor value, two resistors equal to $R_{in}$ were placed in parallel in the feedback loop, effectively achieving the desired resistance.

While this approach is slightly more expensive in terms of the number of components and PCB area, it offers improved accuracy. All resistors in the design share the same resistance value which means that they are typically sourced from the

same production batch, ensuring consistent deviation from the nominal value and thus better overall circuit performance. Additionally, this method minimizes the number of unique part numbers, simplifying the bill of materials (BOM).

### 5.2.1 Filter Design

Due to the non-negligible tolerances of real components, the branches of the adder will not be perfectly balanced, leading to residual noise after signal subtraction. Additionally, even in well-constructed systems, there will always be minor differences in the noise accumulated on one wire compared to the other within the differential pair. These differences necessitate a filtering stage within the differential conditioning circuit.

An important aspect of the filter design is the input frequency of the sine and cosine signals. The frequency of these signals is critical for proper filter design, as it directly impacts the cutoff frequencies required for optimal noise attenuation without signal distortion. Understanding how this frequency is determined requires an examination of the relationship between the motor's speed and its pole pairs.

The number of pole pairs refers to the number of north-south magnetic pairs in the rotor. During each mechanical revolution of the rotor, the position sensors on the stator detect changes in the magnetic field, which are multiplied by the number of pole pairs.

What is obtained is the electrical frequency ($\omega_e$) that is directly related to the SinCos input frequency, and is related to the motor's mechanical speed ($\omega_m$) and the number of pole pairs ($p$) by the following equation:

$$\omega_e = \omega_m \times p$$

To better understand this concept, the motor employed in the HiEFFICENT project will be used as an example.

To determine the SinCos input frequency, the following data was derived from the Elaphe M700 motor specification:

$$\text{Motor pole-pair number: } p = 28$$

$$\text{Maximum speed at 400 V: } \omega_m = 1000 \text{ RPM}$$

The mechanical speed is given in revolutions per minute (RPM). To convert this to revolutions per second (RPS), the following equation is used:

$$\omega_m = \frac{1000\,\text{RPM}}{60 \text{ seconds}} = 16.67 \text{ RPS}$$

Each mechanical revolution corresponds to one electrical cycle per pole pair. Therefore, the frequency of the SinCos signals is the product of the mechanical speed (RPS) and the number of pole pairs:

$$f_{\text{SinCos}} = \omega_m \times p = 16.67 \text{ RPS} \times 28 \text{ pole pairs} = 466.76 \text{ Hz}$$

Thus, the frequency of the SinCos signals for the M700 motor, operating at its maximum speed of 1000 RPM with a 400 V DC-Link, is approximately 467 Hz. This frequency is a key factor to consider in the filter design to ensure it adequately filters out noise while preserving the integrity of the signal processed by the ADC.

To address this, a two-stage filter has been implemented taking as a reference a generic input frequency of 1 kHz. The first stage consists of a first-order low-pass filter integrated directly into the adder. The second stage is a passive low-pass RC filter applied to the output of the generalized adder. This filtering approach ensures effective noise suppression by achieving a -40 dB/dec slope for higher frequencies, reducing unwanted noise while preserving the integrity of the differential signal.

The mathematical derivation for the positive and negative input transfer functions is presented below. This is done using the principle of superposition, where each input is considered active individually, while the others are turned off.

For $V_{in-}$, the transfer function corresponds to that of an inverting amplifier configuration:

$$\frac{V_B}{V_{in-}} = -\frac{Z_2}{R_N}$$

where $Z_2 = R_F \parallel C_2$.

For $V_{in+}$, the computation is performed in two stages: from the input to $V_A$ and from $V_A$ to the output of the adder ($V_B$). A similar derivation can be applied to the other positive input branches.

From the input to node "A":

$$\frac{V_A}{V_{in+}} = \frac{Z_1}{R_1 + Z_1}$$

where $Z_1 = R_2 \parallel R_0 \parallel C_1$.

From node "A" to node "B", the transfer function corresponds to a non-inverting amplifier configuration.

$$\frac{V_B}{V_A} = 1 + \frac{Z_2}{R_N}$$

Thus, the total transfer function for $V_{in+}$ becomes:

$$\frac{V_B}{V_{in+}} = \frac{V_A}{V_{in+}} \cdot \frac{V_B}{V_A} = \frac{Z_1}{R_1 + Z_1} \cdot \left(1 + \frac{Z_2}{R_N}\right) = \frac{Z_1}{R_1 + Z_1} \cdot \frac{R_N + Z_2}{R_N}$$

If:

$$R_N + Z_2 = R_1 + Z_1 \Rightarrow R_N = R_1 \quad \text{and} \quad Z_2 = Z_1$$

Then:

$$\frac{V_B}{V_{in+}} = \frac{Z_1}{R_N}$$

This result holds under the condition that $R_1 = R_N$, which has already been addressed in the adder design discussed earlier. Additionally, the condition $Z_2 = Z_1$ must be satisfied. While the relation $R_0 \parallel R_2 = R_F$ is already ensured by the design of the generalized adder, the requirement $C_1 = C_2$ must also be fulfilled. This is accomplished by selecting both capacitors $C_1$ and $C_2$ to be equal. In the design, the capacitance value has been chosen to be 470 pF.

Thus, this conclusion shows that both inputs share the same transfer function, differing only by a negative sign, and therefore undergo the same filtering effect.

Using the negative input transfer function as an example:

$$\frac{V_B}{V_{in-}} = -\frac{R_F}{R_N} \quad \text{(Passband Gain)} \quad \times \quad \frac{1}{1 + sC_2R_F} \quad \text{(Low-Pass Filter)}$$

The cutoff frequency $f_c$ is given by:

$$f_c = \frac{1}{2\pi C_2 R_F}$$

Substituting the values for $R_F = 11$ kΩ and $C_2 = 470$ pF:

$$f_c = \frac{1}{2\pi \times 11 \text{ k}\Omega \times 470 \text{ pF}} \approx 31 \text{ kHz}$$

The second filtering stage is implemented at the output of the operational amplifier, consisting of an RC low-pass filter formed by a series resistor ($R_3$) and a capacitor ($C_3$). The selected values for this stage are $R_3 = 240\ \Omega$ and $C_3 = 10$ nF. Since $C_3$ is in parallel with $C_4$, the previously mentioned 1 nF capacitor near the microcontroller's analog pin, the total equivalent capacitance is 11 nF, and the expected cutoff frequency is calculated as:

$$f_c = \frac{1}{2\pi \times 240\ \Omega \times 11 \text{ nF}} \approx 60 \text{ kHz}$$

The interaction between the two filtering stages is now considered. The overall transfer function, from the differential input to the ADC, is obtained as the product of the two transfer functions. The second stage does not introduce any additional gain but contributes a second pole, which causes the slope of the Bode plot to increase to -40 dB/decade beyond the cutoff frequency.

The overall transfer function, starting from the negative input, is derived as the product of the transfer functions of the two filters:

$$\frac{V_{out}}{V_{in-}} = \frac{V_B}{V_{in-}} \cdot \frac{V_o}{V_B} = -\frac{R_F}{R_N} \cdot \frac{1}{1 + sC_2R_F} \cdot \frac{1}{1 + sC_3R_3}$$

The canonical form of the second-order low-pass filter transfer function is given as:

$$\frac{\omega_0^2}{s^2 + 2\zeta\omega_0 s + \omega_0^2} = \frac{1}{\frac{s^2}{\omega_0^2} + 2\zeta\frac{s}{\omega_0} + 1}$$

Omitting the pass band gain, the overall transfer function, rewritten in its canonical form, is expressed as:

$$\frac{1}{s^2C_3R_3C_2R_F + s(C_3R_3 + C_2R_F) + 1}$$

From this, the natural frequency $\omega_0$ can be derived by identifying the coefficient of $s^2$, yielding:

$$f_0 = \frac{1}{2\pi\sqrt{C_3R_3C_2R_F}} \approx 43.08 \text{ kHz}$$

The quality factor $Q$ is also determined as:

$$Q = \frac{1}{2\zeta} = \frac{\sqrt{C_3R_3C_2R_F}}{C_3R_3 + C_2R_F} \approx 0.473$$

The quality factor $Q$ characterizes the behavior of the transfer function at the natural frequency. In this case:

$$\left.\frac{V_o}{V_{in-}}\right|_{f_0} = Q = 0.473 \approx -6.5\,\text{dB}$$

This value will be verified through simulation and testing to confirm that the mathematical derivation aligns with the actual behavior of the implemented circuit.

This dual-stage filtering approach effectively attenuates high-frequency noise, ensuring a clean signal at the ADC input without introducing distortion or delay within the operational frequency range.

## 5.3 Simulation

In the simulation of the design, the real component model of the operational amplifier was imported directly into the LTSpice environment from the Texas Instruments website [30]. This step was taken to ensure the simulation reflected the most accurate behavior of the circuit. The remaining components were considered ideal to avoid unnecessary complexity in the analysis.

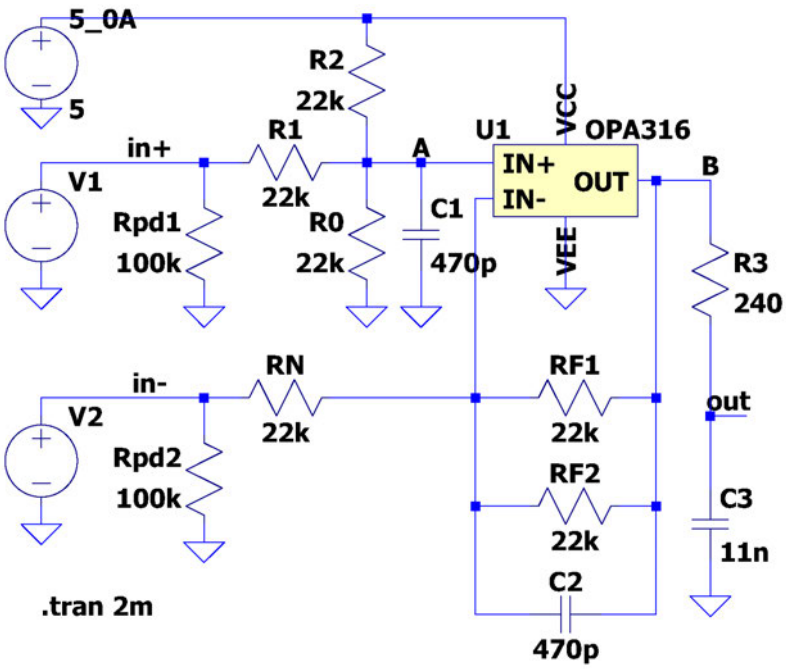


Figure 13: *LTspice scheme of the differential SinCos conditioning circuit.*

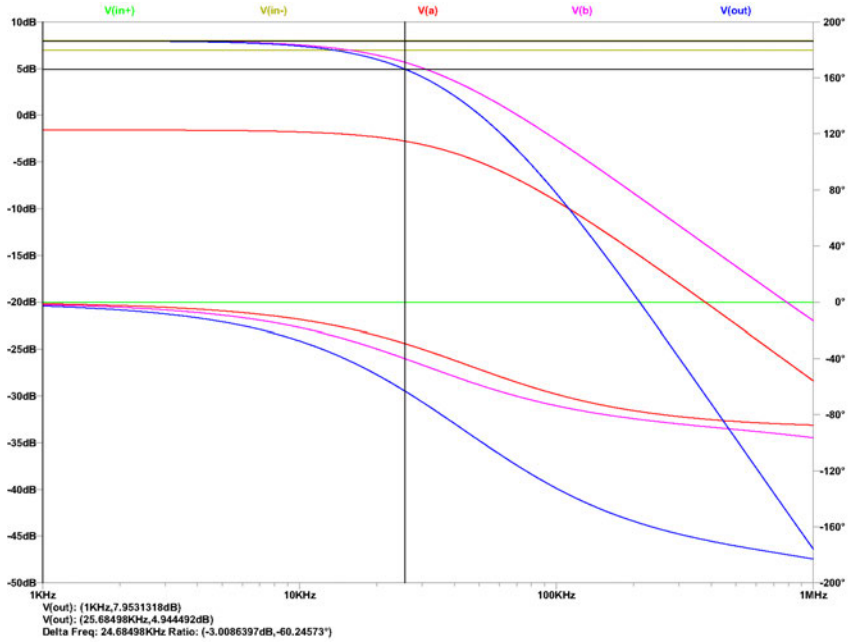


Figure 14: *Frequency domain simulation result.*

The frequency response of the circuit was evaluated with the "AC analysis" command built into LTSpice. From the generated bode diagram, the simulated

-3 dB cutoff frequency was derived to be 25.68 kHz (Fig. 14). This frequency was key in determining the low-pass filtering characteristics of the circuit.

Also, the behavior at the natural frequency was evaluated. The simulation results precisely match the expected behavior of the circuit. At 43.08 kHz the bode diagrams show an attenuation of -6.48 dB pretty close to the -6.5 dB expected value

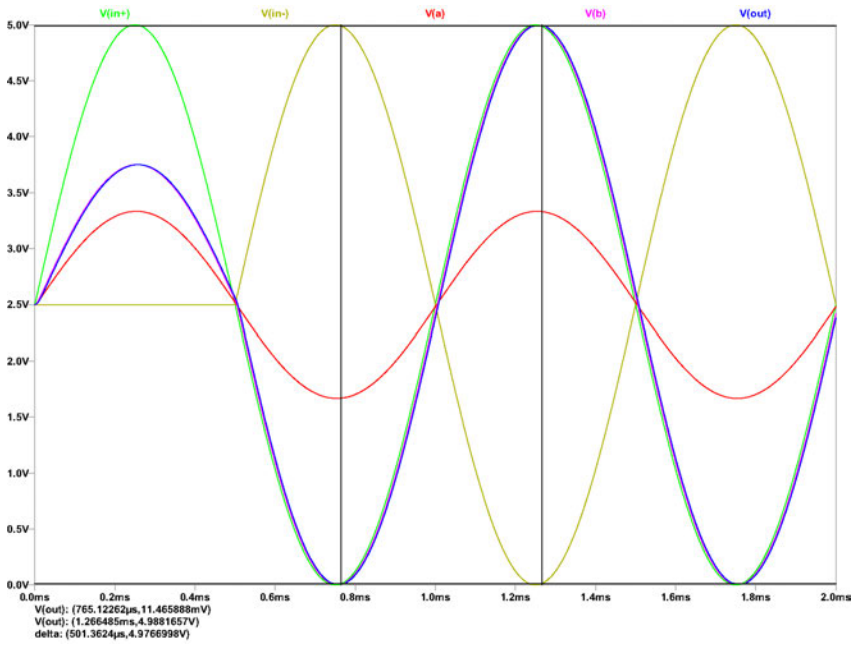


Figure 15: *Time domain simulation results with 1 kHz input frequency.*

The time-domain simulation was conducted using the "Transient" mode in LT-Spice. Repetitive simulations were performed by varying the input signal frequencies to observe the behavior of the output waveform under different conditions. A benchmark input frequency of 1 kHz was selected as a representative case to evaluate the filter's behavior in the passband.

As shown in Fig. 15, the output amplitude at 1 kHz in the simulation was approximately 4.98 V, which closely matches the input amplitude of 5 V. The -3 dB amplitude was calculated by multiplying the input amplitude by the factor $\frac{1}{\sqrt{2}}$, resulting in a value of approximately 3.54 V.

At 25 kHz, as depicted in Fig. 16, the resulting output amplitude closely aligns with the calculated -3 dB value, with a minor deviation (3.63 V vs. 3.54 V). This slight difference is consistent with the expected frequency response because the input frequency of 25 kHz is slightly below the cutoff frequency. As a result, the observed amplitude is marginally higher than the ideal -3 dB value.

In conclusion, this small mismatch does not contradict the circuit's calculated cutoff frequency from the AC analysis. Rather, it demonstrates consistency between the time-domain and frequency-domain simulations, validating the filter behavior.

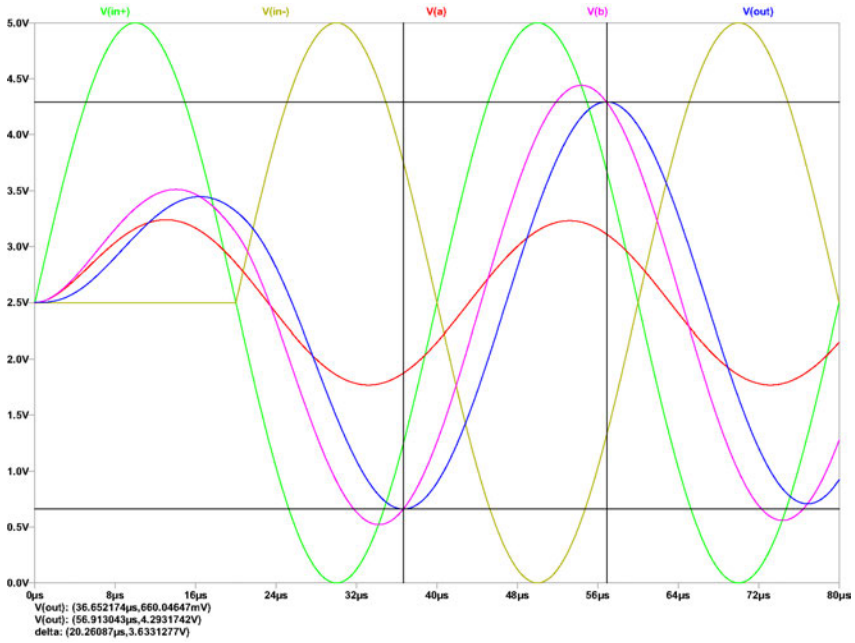


Figure 16: *Time domain simulation results with 25 kHz input frequency.*

A comparison of the two time-domain simulations reveals significant differences in signal behavior at the two frequencies. At 1 kHz, the input and output signals are nearly indistinguishable, indicating that the circuit operates within the passband without introducing any noticeable attenuation or phase delay. However, at 25 kHz, a clear attenuation and delay in the output signal relative to the input can be observed.

The measured delay at 25 kHz was approximately 6.9 $\mu$s. To determine the phase shift between the input and output signals, the delay was divided by the period of the input signal and then multiplied by 360 degrees. This yielded a phase shift of approximately 62°, which aligns well with the AC analysis (Fig. 14), where the phase shift at 25 kHz was measured at 61.75°. This close agreement between the time-domain and frequency-domain analyses confirms the consistency and accuracy of the measurement results.

## 5.4 Testing

A measurement was conducted on the physical circuit to validate the expected behavior of the components and the overall system performance. The purpose of the test was to ensure that the measured results align with theoretical predictions and simulations conducted earlier.

The measurement was conducted with input sine waves generated by the signal generator at frequencies of 1 kHz and 25 kHz to assess the performance of the

circuit. The oscilloscope was used to observe the output waveforms and compare them to the expected behavior.

At 1 kHz, the circuit exhibited a slight amplification behavior, which resulted in a clamped output waveform when the input was set to a 5 V peak-to-peak amplitude. The measurement demonstrates that the actual input range is less than the nominal one of 0-5 V. However, the reduced range does not affect normal operation since input waveforms from the SinCos sensors usually do not fully utilize the entire dynamic range.

For example, the Elaphe M700 motor, as previously discussed, uses SinCos sensors that operate with a dynamic range of $3.6\,\mathrm{V} \pm 0.8\,\mathrm{V}$ even though they are supplied at 5 V.

Therefore, to better measure and test the circuit, the amplitude of the two input signals was reduced to achieve a non-distorted sinewave at the output. The observed amplification was calculated as the ratio between the output amplitude and the input amplitude, and it was evaluated as follows:

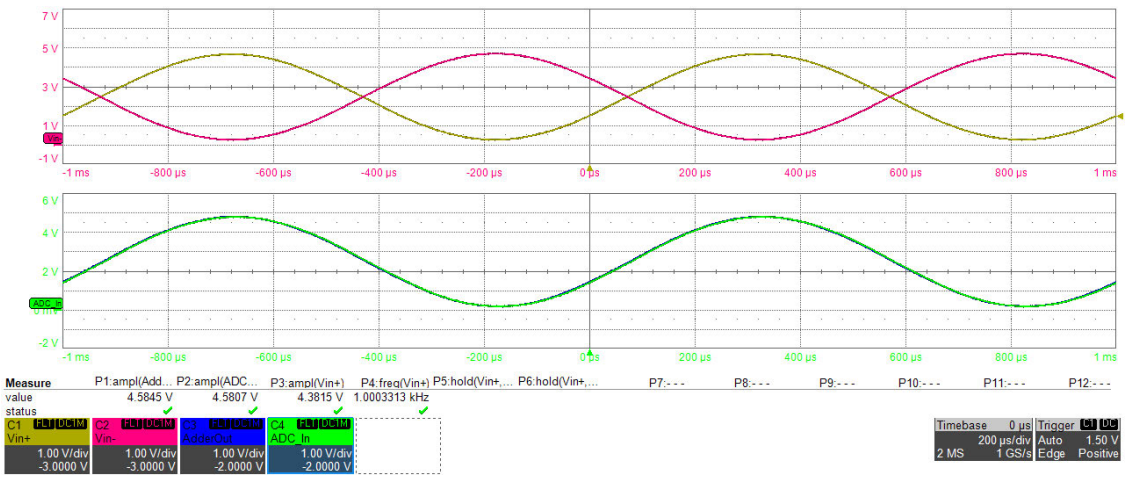


Figure 17: *Oscilloscope capture at 1 kHz input frequency; on the upper graphic differential inputs, on the lower graphic the output of the adder and the ADC input.*

From the oscilloscope measurement in Fig. 17, the input amplitude $V_{in+}$ is approximately 4.38 V, and the output amplitude $V_{ADC}$ is approximately 4.58 V.

The amplification factor $A_v$ is calculated as:

$$A_v = \frac{\text{Output Amplitude}}{\text{Input Amplitude}} = \frac{4.58\ \text{V}}{4.38\ \text{V}}$$

Thus, the amplification factor is:

$$A_v \approx 1.045$$

At 25 kHz, the circuit exhibited the expected behavior, with the output waveform closely matching both theoretical predictions and simulation results. The inputs were once again driven with the full voltage swing, ranging from 0 to 5 volts. The measured output amplitude of 3.586 V confirmed the expected -3 dB attenuation, aligning almost perfectly with the simulated value of 3.63 V.

The oscilloscope capture of the waveform is shown in Fig. 18, illustrating the accuracy of the measurement and the consistency with the simulation findings.

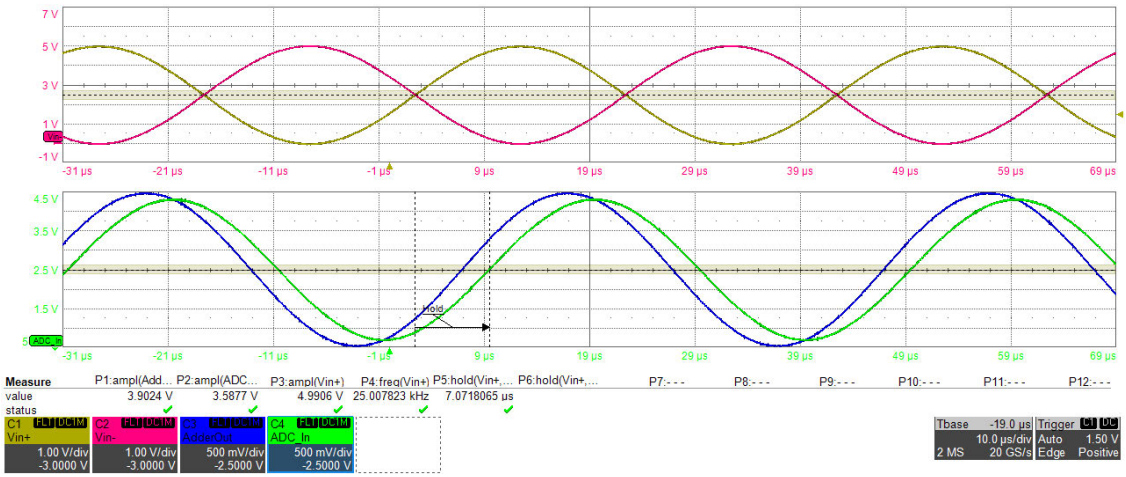


Figure 18: *Oscilloscope capture at 25 kHz input frequency; on the upper graphic differential inputs, on the lower graphic the output of the adder and the ADC input.*

The delay measured during the simulations at 25 kHz was confirmed by the measures taken on the oscilloscope. The delay found in the real circuit is 7 $\mu$s very close to the 6.9 $\mu$s of the simulation.

A frequency-domain analysis was conducted using the Analog Discovery 2, a USB oscilloscope, to measure the actual frequency response of the circuit. The Analog Discovery 2 produces Bode plots via the network analyzer function, exploiting the internal function generator, at selected starting and stop input frequencies, amplitude, and number of samples. The tool automatically sweeps through the defined frequency range, measuring the circuit's output and calculating the gain of the transfer function between the input and output. The results are then plotted as a frequency-based Bode plot.

Due to the limitation of selecting only one input as the frequency sweep source, it was not possible to measure the frequency response when the circuit was configured as a differential amplifier. To approximate the desired behavior, the positive input was set as intended to 5 V peak-to-peak with a 2.5 V offset while the negative input was supplied with a DC voltage equal to 2.5 V to counterbalance the offset on the positive branch.

The results are shown in Fig. 19, where the blue curve represents the overall

circuit response, and the yellow curve depicts the filtering effect observed after the first stage (the output of the adder).

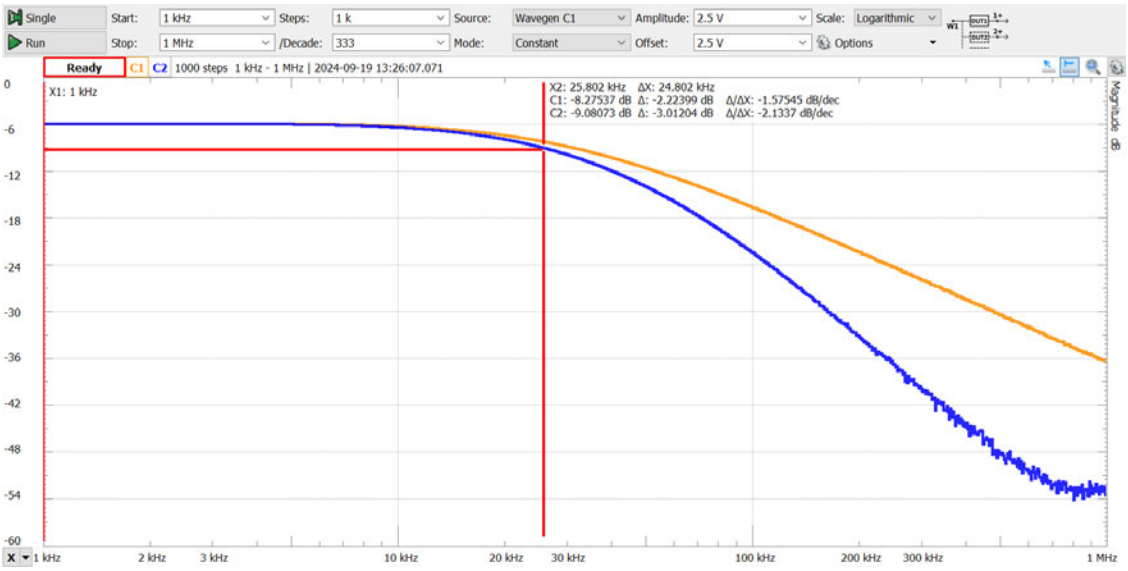


Figure 19: *Frequency response measured with Analog Discovery 2: Blue curve shows full circuit, yellow curve shows first filtering stage.*

The cutoff frequency for the complete circuit (blue curve) was measured at approximately 25.8 kHz, which is just above the simulated value but still very reasonable, accounting for component tolerances and parasitic.

The observed discrepancy between the simulated and measured Bode diagram amplitude is due to the difference in how the magnitude is reported by the tools used. Specifically:

- **LTSpice** reports the magnitude as the peak voltage at the output. This means that the value displayed in the Bode plot (8 dB in the passband) directly corresponds to the actual output voltage (2.5 $V_{\text{peak}}$).
- **Analog Discovery 2** calculates the magnitude as the ratio of the output voltage to the input voltage. In this case, the reported value (-6 dB in the passband) represents the transfer function $\frac{V_{out}}{V_{in}}$, which reflects the relationship between the input and output signals $\left(\frac{2.5\ \text{V}}{5\ \text{V}} = 0.5\right)$.

Because of this difference in reference, the amplitude at 1 kHz (and other frequencies) appears higher in the LTSpice simulation, as it represents the absolute output voltage. On the other hand, the Analog Discovery 2 tool reports the normalized transfer function, which inherently takes the input signal into account. Taking this difference in the results reports, the measured and the simulated Bode plots are well aligned.

Also, an evaluation of the natural frequency was performed. the results found by testing the real circuit are pretty close to the simulation. the gain of the whole conditioning circuit transfer function at $\approx$ 43.1 kHz is found at -6.54 dB, a value that agrees with the simulation results.

The design validation performed by the simulation of the circuit and the testing of the board confirmed the precise compliance to the design expectation, aligned with the overall system requirements.

# Chapter 6

# Digital Position Sensors

## 6.1 Overview

There are several methods by which a digital sensor can provide the rotor's position to the microcontroller, each with varying levels of complexity and precision. One of the simplest methods involves the binary output of a latching device, such as a Hall effect sensor, combined with other sensors placed on different phases of the motor. This setup usually employs three Hall sensors, one per motor phase, to monitor the rotor's magnetic field and determine its position.

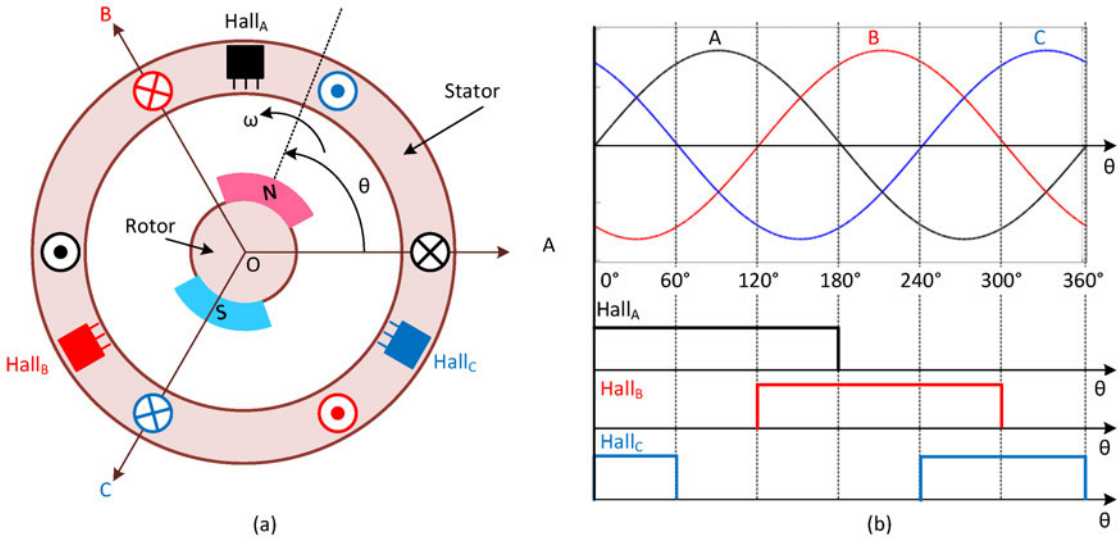


Figure 20: *Six-Step Motor Commutation Control Scheme for a PMSM motor with one pole-pair [2].*

In a basic implementation, each Hall sensor outputs either a high (H) or low (L) signal, indicating whether the North or South pole of the rotor magnet was the last to pass by the sensor. The three Hall sensor outputs form a 3-bit binary code,

where each unique combination corresponds to a specific step in the commutation sequence. The commutation sequence is the predefined order in which the inverter switches are activated to energize the appropriate motor windings, ensuring the rotor moves smoothly and efficiently. This simple coding scheme enables the microcontroller to determine which motor phase needs to be energized next to drive the rotor in the desired direction.

An important distinction is that with analog sensors, the resolution of position sensing is determined by the number of samples acquired by the ADC and is therefore not dependent on the sensor itself. In contrast, with digital sensors, the resolution is finite and limited to the number of sensing elements [27].

Taking the Elaphe M700 motor as an example, assuming it is equipped with 3 Hall effect digital latching sensors, the achievable resolution is obtained by dividing the full turn angle by the product of the number of pole pairs and six (the number of possible combinations of the three inputs).

$$\text{MaxRes} = \frac{360^\circ}{28 \times 6} = 2.14^\circ$$

The simplicity of this method makes it suitable for many applications, especially in cost-sensitive designs, as it requires minimal processing power and can operate efficiently even with low-resolution sensors. However, for applications with high-speed motors, where typically the pole pair count is smaller, Hall effect-based sensors require a large number of Hall elements to achieve sufficient accuracy, which increases the costs [11].

## 6.2 Conditioning Circuit Design

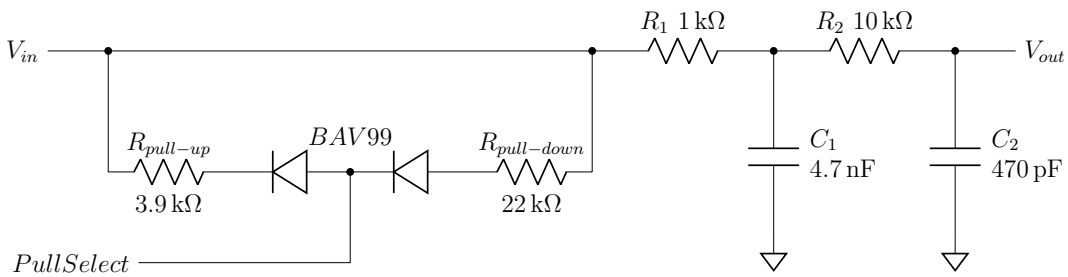


Figure 21: *Circuit diagram showing the adopted solution for conditioning the digital position input signals.*

When using latching Hall effect sensors, the frequency of the digital signals on the microcontroller's input channels is determined by the electrical frequency of the motor and is expressed in the same manner as discussed in the analog sensors conditioning chapter.

A conditioning circuit is still required to properly interface digital position sensors to reject noise that could result in errors in the data transmission. The circuit implemented on the board has been designed to properly handle the digital signal in the intended frequency range while effectively rejecting noise. To achieve this, a second-order low-pass filter is employed, which provides a double-pole characteristic. This is implemented by cascading two RC low-pass filters with the same cutoff frequency.

The transfer function can be derived as follows:

$$\frac{V_{out}}{V_{in}} = \frac{C_1 \parallel (R_2 + C_2)}{R1 + C_1 \parallel (R_2 + C_2)} \cdot \frac{C_2}{R_2 + C_2}$$

which in the Laplace domain become

$$\frac{1}{s^2 R_1 R_2 C_1 C_2 + s\left[R_1 (C_1 + C_2) + R_2 C_2\right] + 1}$$

From this expression, similar to the analysis of the analog sensors, the natural frequency and quality factor of the circuit can be identified. By design, the two poles introduced by the RC stages are placed at the same frequency, resulting in a natural frequency that coincides with the cutoff frequency of both filters.

Since the cutoff frequency of a single-stage RC low-pass filter depends on the product $R{\cdot}C$, the implementation of the two stages can be done with either identical values for both stages or with different component values that maintain the same RC product. If both stages are designed to be identical, the quality factor of the total transfer function will be $Q = \frac{1}{3}$. This is suboptimal, as it results in an attenuation of -9.54 dB at the designed cutoff frequency.

To achieve better performance, the two stages can be designed with the same RC product but with component values that differ by a decade. This approach significantly improves the quality factor, and it was the solution chosen for implementation on the board. Specifically, the values chosen are $R_1$=1 kΩ and $C_1$=4.7 nF for the first stage, and $R_2$=10 kΩ and $C_2$=470 pF for the second stage. The resulting natural frequency can be calculated as follows:

$$f_0 = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}} \approx 33.86\,\text{kHz}$$

The quality factor $Q$ is determined as:

$$Q = \frac{1}{2\zeta} = \frac{\sqrt{R_1 R_2 C_1 C_2}}{R_1 (C_1 + C_2) + R_2 C_2} = \frac{10}{21} \approx 0.476$$

This quality factor corresponds to an attenuation of -6.44 dB at the natural frequency, which is a significant improvement compared to the previous solution. It is important to note that, when cascading two passive RC filters with the same cutoff frequency, the maximum achievable quality factor is $\frac{1}{2}$. This means that the

chosen design, where the component values of the two stages differ by a factor of 10, already provides a substantial improvement over a design where both stages are identical.

This design solution provides proper filtering of high-frequency noise while allowing the digital signal of interest to pass through without any considerable data integrity problems.

Additionally, the way sensors drive the digital line must be considered, as some may be push-pull, while others may be open drain configurations. To maintain flexibility, a selectable pull resistor circuit is implemented. The selection of the pull resistor is controlled through a dedicated line and two diodes. The configuration of this line (high or low) determines which diode is activated, and consequently, which resistor is used to pull the external digital line.

In the push-pull configuration, no pull-up resistor is required, as the sensor is capable of driving the line both high and low. In this case, the circuit should include a weak pull-down resistor, with a sufficiently high value to avoid interfering with the sensor's driving capability. The pull-down resistor provides a diagnostic feature: in the event of disconnection or malfunction of the sensor, the resistor will pull the line low, allowing the microcontroller to detect the fault condition.

In the open-drain configuration, the sensor can only pull the line low, while the high state is maintained by an external pull-up resistor. The pull-up resistor must have a sufficiently low resistance to ensure fast signal transitions. However, since the sensor signal originates from the external environment, potential faults, such as a short to the battery voltage, must be considered. This issue is addressed by placing a diode in series with the pull-up resistor, which prevents reverse current flow during a short-to-battery event. As a result, this configuration eliminates the limitation on the pull-up resistance value while providing protection against fault conditions.

Nevertheless, the pull-up resistor value is still constrained by several factors, including the power ratings of both the diode and resistor. Lower pull-up resistance values can result in overcurrent conditions in the sensor and the component driving the pull-select line if the current exceeds their rated capacity. To mitigate this risk and minimize unnecessary power dissipation, a pull-up resistance value of 3.9 kΩ was chosen for the final design. This value strikes a balance between achieving fast signal transitions and preventing sensor overload.

## 6.3 Simulation

A simulation of the circuit was conducted using an NMOS transistor, specifically the BS170, to emulate the output of an open-drain sensor. Additionally, a model of the BAV99 diode was imported from the Nexperia website [31] to accurately replicate the behavior of the real circuit.

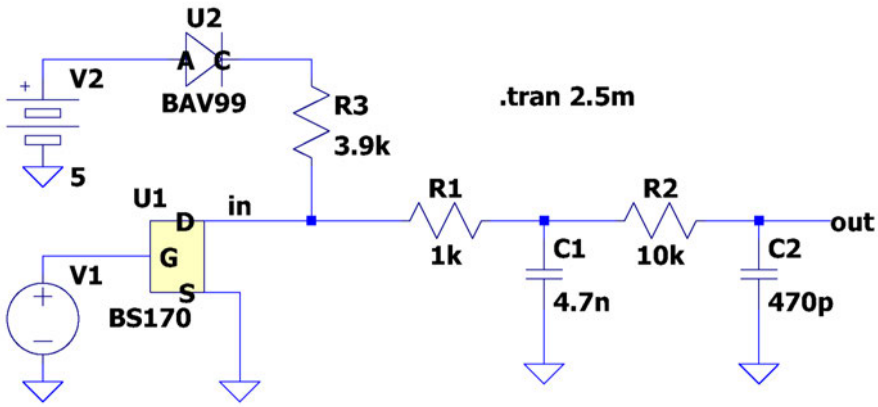


Figure 22: *LTspice scheme of the digital position conditioning circuit.*

Figure 22 presents the electrical schematic as configured in the LTSpice simulation environment. The initial simulation involved a transient analysis of the circuit, operating at a reference input frequency of 1 kHz. The results demonstrated that the circuit performed as expected.

The output of this transient simulation is illustrated in Figure 23.

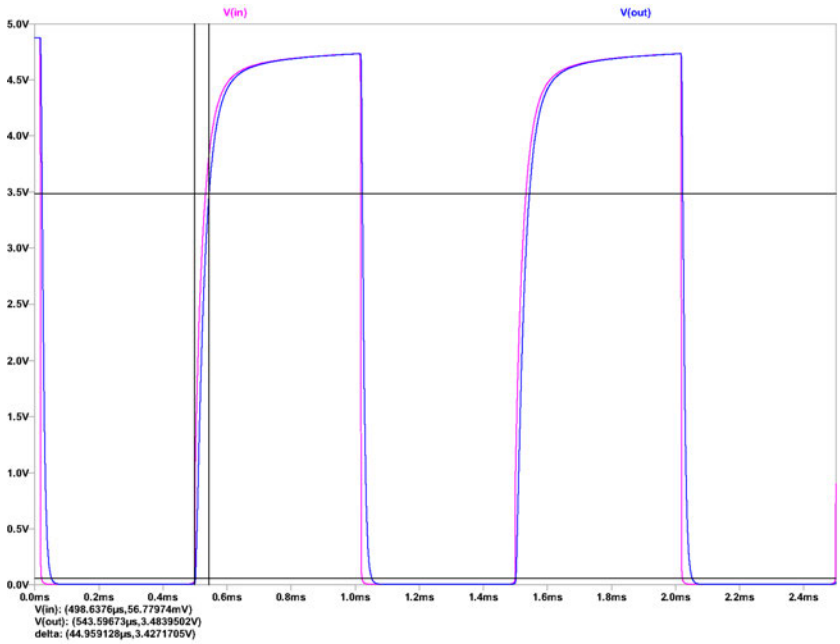


Figure 23: *Time domain simulation results with 1 kHz input frequency.*

During the simulation, the delay introduced by the circuit was measured, with particular attention to the rise time, where the pull-up resistor plays a critical role

in the speed of the transition. The delay interval was measured from the beginning of the sensor's signal transition to the point where the logic level on the microcontroller side reached the "$V_{IH}$" (input high voltage) threshold for CMOS/Automotive logic, which is 3.5 V according to standard specifications. The measured delay was approximately 45 $\mu$s, which represents around 4.5% of the input signal's period. While this is relatively high, I&M experience has confirmed that this delay does not compromise the precision of the position readings, ensuring accurate performance during standard operation.

The falling-edge delay was also measured at approximately 14 $\mu$s. This interval was taken from the start of the falling edge on the sensor side to the point where the logic level reached the "$V_{IL}$" (input low voltage) threshold on the microcontroller side, which is 1.5 V in accordance with CMOS/Automotive logic standard.

An AC analysis was performed to verify the actual cutoff frequency of the circuit using the ".ac" function in LTSpice. For this simulation, the voltage generator $V_1$ was directly connected to the input of the circuit, bypassing the NMOS BS170 transistor. The simulation generated a Bode plot with a frequency range from 1 kHz to 1 MHz.

The -3 dB cutoff frequency was measured at approximately 20.36 kHz, which is, as expected, lower than the natural frequency of the circuit. The Bode plot also showed an attenuation of approximately -6.44 dB around the natural frequency $f_0$, which aligns closely with the expected theoretical value.

The simulated Bode plot result is shown in Fig. 24:

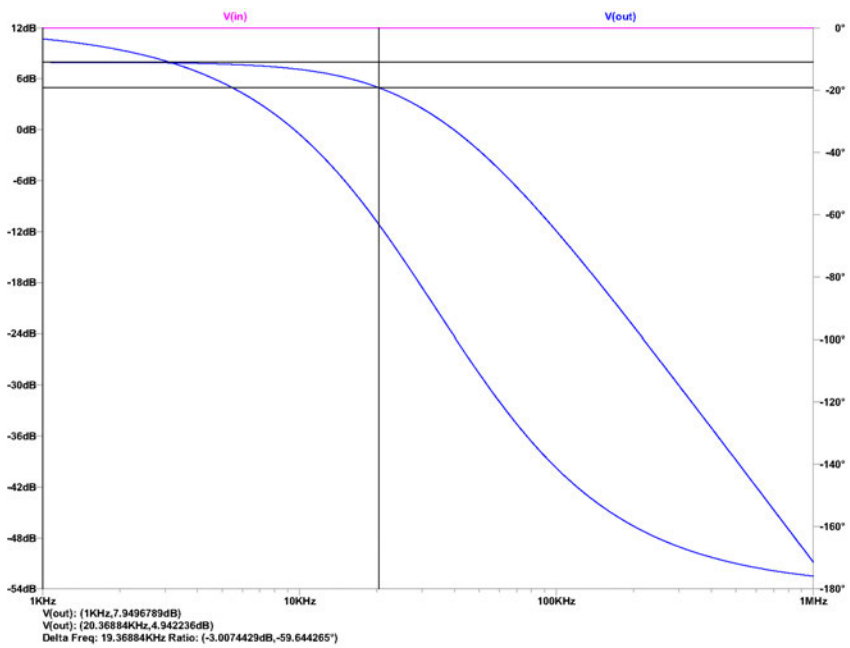


Figure 24: *Frequency domain simulation results.*

## 6.4 Testing

To validate the actual behavior of the circuit, several tests were performed on the physical board to ensure proper functionality.

The frequency response of the circuit was measured to verify its filtering performance. The results are shown in Figure 25.

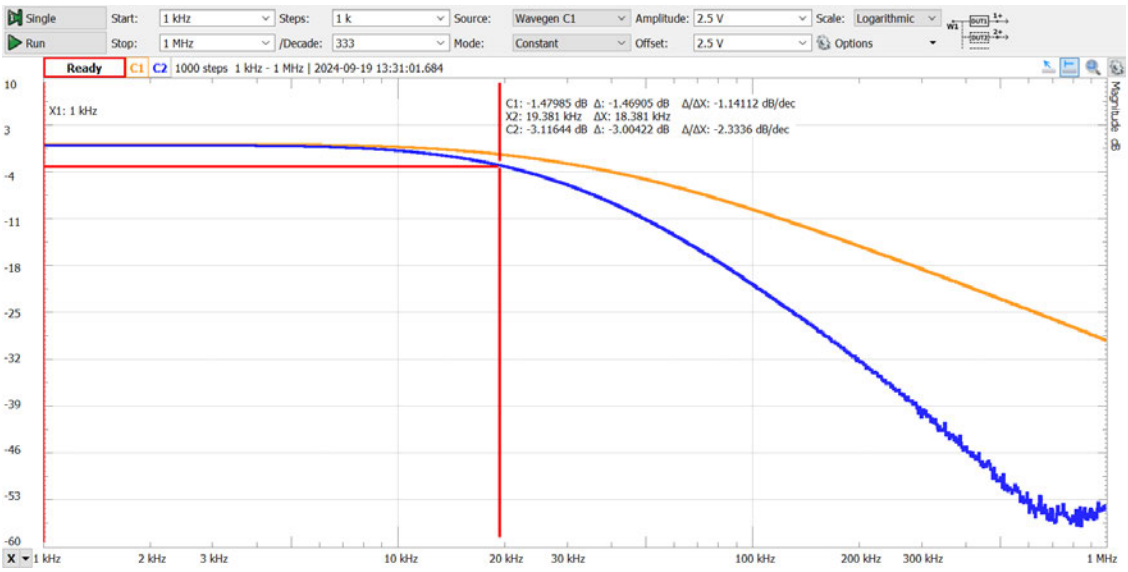


Figure 25: *Frequency response measured with Analog Discovery 2: Blue curve shows full circuit, yellow curve shows first filtering stage.*

The blue curve represents the output of the conditioning circuit, while the yellow curve shows the response of the first filtering stage. It is evident that the filter achieved a post-passband slope of -40 dB/dec. The measured cutoff frequency was slightly lower than the simulated one, measured at 19.3 kHz. This deviation is likely due to extra parasitic capacitances and tolerances of the physical components used in the circuit.

The natural frequency attenuation was measured at -6.9 dB, which, while slightly lower than the expected value, is consistent with prior measurements indicating a lower cutoff frequency.

A time-domain analysis was performed using the BS170 transistor to emulate the open-drain output of a digital position sensor. The NMOS transistor was driven at a frequency of 1 kHz, and the pull-select line on the board was set to 5 V to engage the pull-up resistor. The observed behavior was captured on the oscilloscope and is displayed in Figure 26. In this figure, the magenta waveform represents the input signal applied to the gate of the transistor, while the blue waveform shows the filtered output signal.

By zooming in on the time axis, the real delay between the sensor's commutation

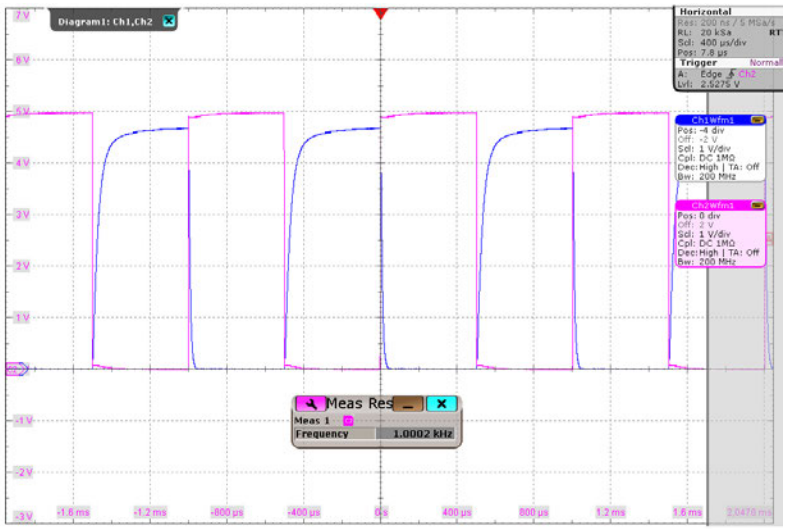


Figure 26: *Oscilloscope capture at 1 kHz input frequency.*

and the time when the logic level on the microcontroller reaches the minimum value for a valid reading was measured. The measurements were taken on both the rising and falling edges of the commutation, allowing for comparison with the simulated results.

The results for the rising edge delay and the falling edge delay are shown in Figure 27.

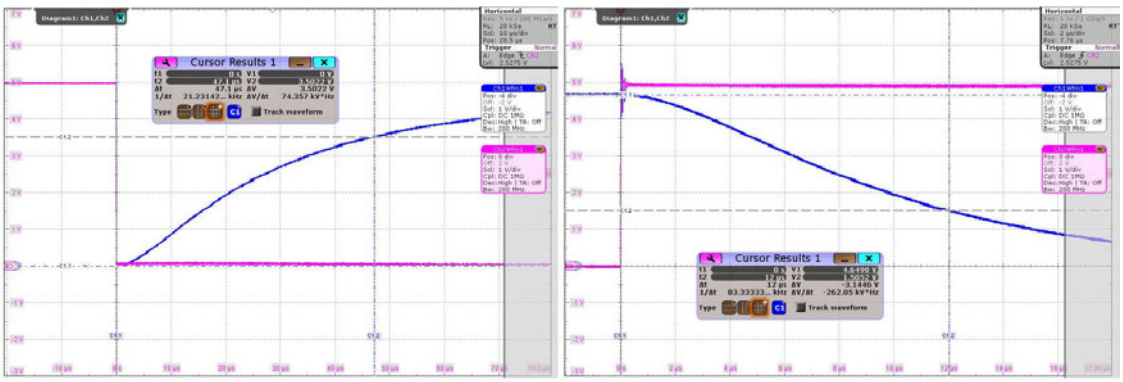


Figure 27: *Oscilloscope capture of rising and falling edge delay measurements.*

As expected, the delay during the rising phase was significantly larger than during the falling edge. The measured delays were: $t_{\text{rise}} = 47\,\mu\text{s}$ and $t_{\text{fall}} = 12\,\mu\text{s}$. These results show minor deviations from the simulations remaining within acceptable limits.

In conclusion, the measurements on the physical board confirmed the good behavior of the circuit under the intended operating conditions.

## 6.5 Synchronous Serial Interface

Another method through which digital position sensors can communicate with a microcontroller is by using dedicated communication protocols. One of the most commonly used is the Synchronous Serial Interface (SSI).

The SSI protocol is a widely used method for transmitting position data from encoders to microcontrollers. It offers a synchronous form of communication, where data is transmitted in sync with a clock signal provided by the microcontroller. This synchronous nature allows for better control over the timing and speed of data transmission.

One of the key advantages of SSI is its use of well-established physical communication standards such as RS-422 or RS-485 [32]. These standards offer robust noise immunity and are well-suited to automotive environments where high levels of electromagnetic interference (EMI) can occur. The use of differential signaling in SSI, with separate twisted-pair lines for the clock and data signals, further enhances its resistance to interference, ensuring reliable data transmission even in challenging conditions.

In operation, the SSI master initiates communication by sending a clock signal to the encoder. The encoder, in response, transmits the position data serially, bit by bit, starting with the most significant bit (MSB). In addition to position data, many SSI encoders transmit error checker bits at the end of the data transmission sequence. These error checker bits are used to verify the integrity of the transmitted data, ensuring it has not been corrupted during transmission.

A notable feature of SSI is its use of Gray coding for position data [32]. Gray code is a binary numeral system where only one bit changes between successive values, reducing the chance of errors during state transitions. In fast-moving systems, such as motors or robotics, this feature is particularly important because it minimizes the risk of erroneous readings caused by simultaneous bit changes.

Overall, the SSI protocol provides a robust and flexible approach for transmitting absolute position information, making it ideal for applications requiring high precision and reliability. Its synchronous communication method, strong noise immunity, error-handling mechanisms, and the use of Gray coding make it particularly suited for demanding environments. In the context of automotive electric motors, SSI ensures efficient and accurate communication of position data, allowing for precise motor control and contributing to the overall reliability and performance of the system.

The SSI compatibility is ensured by the integration of the SN65LBC179QDR IC from Texas Instruments on the board. This IC is a low-power differential line driver and receiver pair capable of handling the differential signals required by SSI while communicating in single-ended mode with the microcontroller. One of its key features is the ability to support full-duplex operation, as the driver's differential outputs and the receiver's differential inputs are connected to separate terminals.

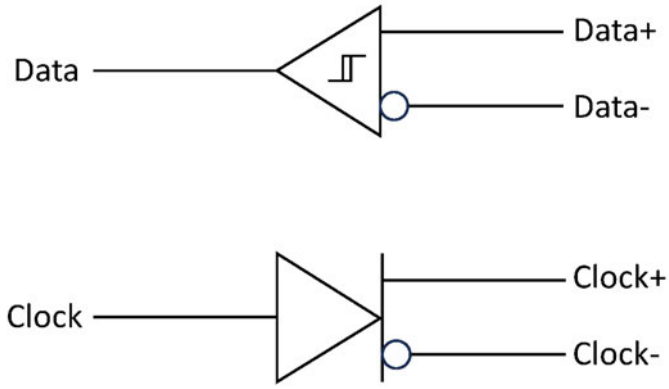


Figure 28: *SSI transceiver logic diagram [3].*

This characteristic is essential for the proper functioning of the SSI protocol, which is why this IC was selected.

A 120 Ω termination has been implemented on the receiver's differential inputs using two 60.4 Ω resistors in series. The necessity of termination depends on the characteristic impedance of the transmission line used to connect the sensor to the board. For example, in the case of the two communication standards mentioned earlier, RS-422 requires termination only at the end of the line opposite to the driver, while RS-485 requires termination resistors at both ends [33]. The implemented design allows for flexibility, providing the option to mount or not the termination impedance depending on the requirements of the final application. Additionally, in the event a different physical standard is used, the resistor values can be adjusted to match the characteristic impedance of the transmission line, ensuring proper signal integrity.

# Chapter 7

# Programmable Inputs

To make the control board adaptable to a wide range of applications, it was designed with broad compatibility in mind. While position sensor feedback is crucial to the motor control strategy, the board also needs to interact with other generic sensors and subsystems that may communicate using different protocols or signal types. To address this, the board incorporates three types of interfaces for external inputs, each capable of handling analog signals, digital on/off states, and frequency-based signals such as PWM. All of these interfaces are software-programmable, which significantly enhances the board's flexibility and adaptability.

## 7.1 Shift Registers

As previously mentioned, each circuit is programmable, allowing the configuration of inputs to accept both analog and digital signals. This flexibility introduces significant challenges in designing the conditioning circuits, as different signal types require distinct processing.

In designing configurable hardware, a significant number of configuration signals are required to accommodate the various input types. Directly using microcontroller pins to handle all these signals would quickly exhaust the available I/O resources. To overcome this challenge, shift registers were implemented. By using shift registers, multiple configuration signals can be controlled with just a few microcontroller pins through serial communication, reducing the hardware complexity while still allowing for full programmability of the board's inputs.

The shift registers used in this design are SN74LV595AQPW, which do not have a native SPI interface. Instead, they operate using basic serial input and clock signals, requiring careful consideration when interfacing with the SPI bus to ensure proper operation, especially when communicating with other peripherals on the SPI bus.

Figure 29 illustrates the internal structure of the shift register. The integration

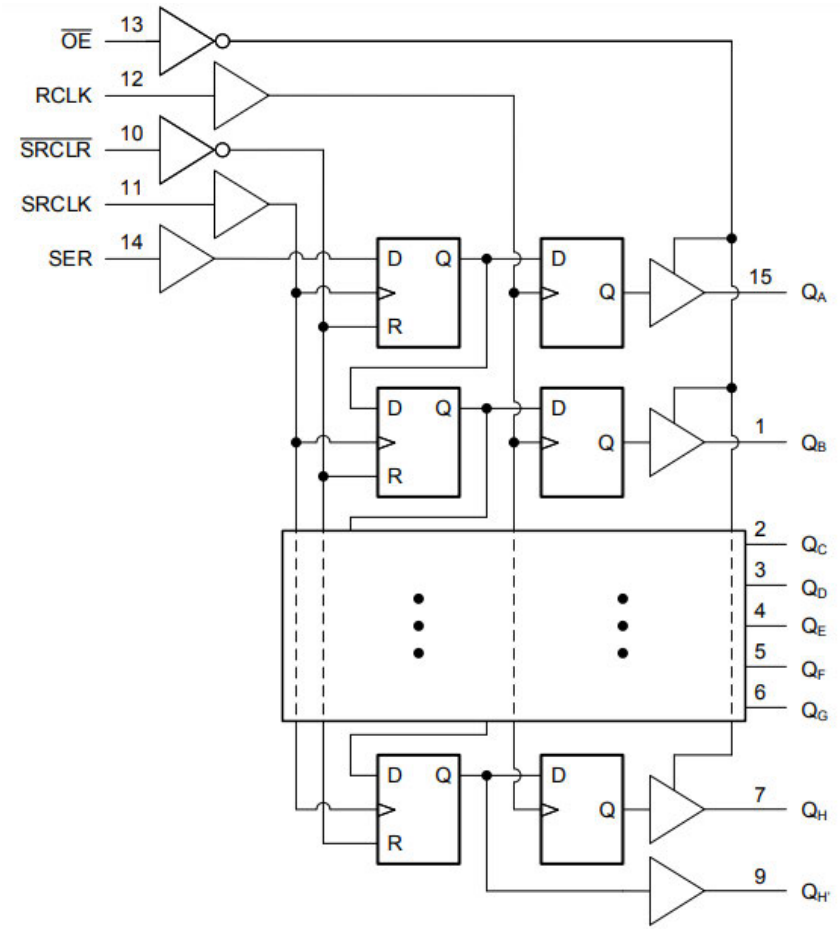


Figure 29: *Shift Register Internal Diagram [4],*

of this IC into the board design involves connecting the **SER** (serial input) pin to the MOSI line and the **SRCLK** (shift register clock) pin to the SPI clock. With each clock pulse, data in the shift register shifts by one position, with new data being stored in the first position. The **RCLK** (register clock) pin is connected to the chip select (CS) signal, which controls when the stored data is transferred to the output pins. During SPI communication, the CS (active low) remains asserted, keeping the outputs unchanged. Once the communication is complete and the CS signal is deactivated, the data is latched and transferred to the output pins, allowing the shift register to output the newly stored data.

All the shift registers share the same chip select (CS) signal because they are connected in a daisy-chain configuration. In this setup, the serial data output of one shift register is directly connected to the serial data input of the next register in the chain. As a result, data is shifted through each register sequentially, with the output of one register feeding the input of the next. This allows a single serial data stream to configure all the shift registers efficiently, reducing the number

of control lines needed and enabling control of multiple registers using minimal microcontroller resources. The serial data output from the last shift register (QH') is then sent back to the microcontroller via the SPI MISO line.

Because the shift registers lack a native SPI interface, two tri-state buffers are needed to prevent communication errors when the SPI bus is used for other devices.

One buffer is placed on the MISO line, ensuring that the MISO line is released when other devices need to use the SPI bus. This effectively prevents any unintended interference from the shift registers, which could otherwise continue to drive the line even when the CS is disabled.

Another tri-state buffer is placed on the clock line. This buffer prevents unintended shifts in the shift register data when the SPI clock is being used for other devices. Although the outputs remain unchanged, the internal flip-flops still shift data on each clock pulse. This can lead to unknown data within the shift registers, which is undesirable.

Even with the buffer on the clock line, an extra clock signal transition can occur at the end of transmission, depending on the SPI configuration. This can lead to an unintended extra shift in the data stored within the shift registers. To avoid this, it is essential to configure the SPI clock polarity (CPOL) and clock phase (CPHA) correctly to ensure proper synchronization with the shift registers.

These two parameters control how the clock signal interacts with the data during transmission, and each can be set to either 0 or 1. Their functions are as follows:

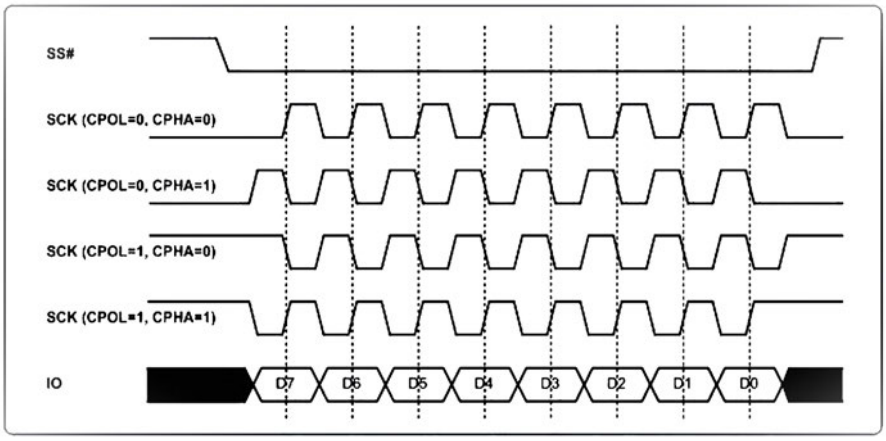


Figure 30: *SPI timing diagram showing clock behavior for different CPOL and CPHA configurations [5].*

- **Clock Polarity (CPOL):** This parameter defines the default or idle state of the clock signal when no data is being transmitted.

  If CPOL is set to 0, the clock signal remains low (0) when idle.

  If CPOL is set to 1, the clock signal remains high (1) when idle.

- **Clock Phase (CPHA):** This parameter determines when the clock transitions from its idle state to its active state during data transmission. Specifically, CPHA defines the point in the transmission cycle when data is sampled.

  If CPHA is set to 0, the clock transition occurs in the middle of the data transmission, so data is sampled on the leading edge (from idle to active).

  If CPHA is set to 1, the clock transition from idle to active occurs at the beginning of the data transmission, meaning that data is sampled on the clock's trailing edge (from active to idle).

The shift register clock is triggered by the rising edge, which means that to avoid an extra shift at the end of the communication when the chip select signal is disabled, the clock signal must not exhibit a rising transition. To ensure this behavior, a pull-down resistor is placed after the clock buffer, keeping the shift register's clock line at a low logic level when not driven. This hardware design, combined with the configuration of CPOL and CPHA ensures the desired communication behavior without unintended data shift at the end of the transmission.

CPOL and CPHA settings can be adjusted depending on the peripheral the SPI is communicating with, but this design allows interaction with the shift registers without the need for explicit clock parameter configuration. This solution ensures compatibility and correct operation with the default settings of CPOL = 0 and CPHA = 0, enabling the microcontroller to efficiently manage the shift registers, despite their lack of a native SPI interface.

## 7.2 Rereading Pull-Up Voltage

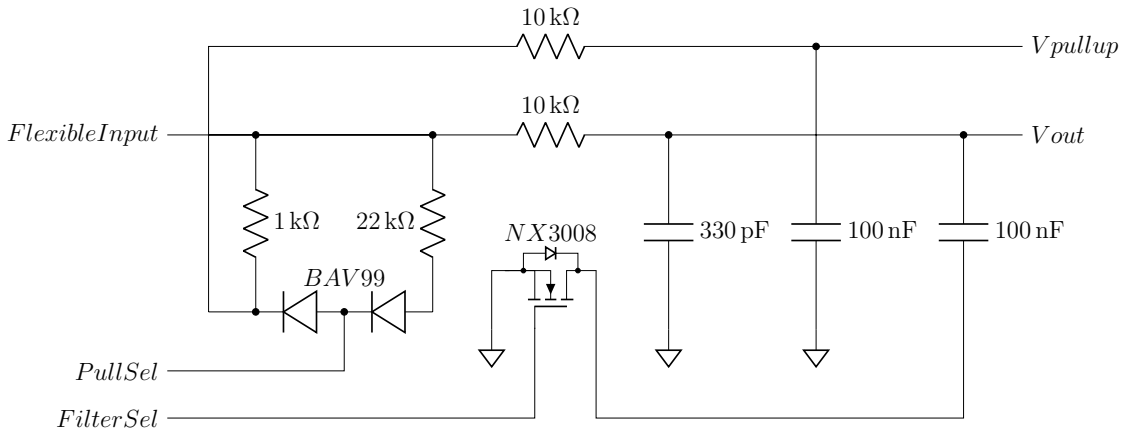


Figure 31: *Circuit diagram showing the flexible input "ReReading Pull-Up Voltage".*

This circuit design provides flexibility in how the input signal is conditioned,

with options to adjust pull-up/down resistors and filtering behavior. Here's a breakdown of how the circuit operates:

The circuit provides a flexible configuration for selecting different pull-resistor values. Specifically, the implemented design uses a "strong" pull-up with a low resistance value (some kΩ) and a "weak" pull-down with a higher resistance value (typically tens of kΩ).

This flexibility allows the circuit to be tailored to the specific requirements of the connected sensor or signal source. By programming the output of the shift register via SPI, which is connected to the PullSel line, it is possible to select the desired configuration by means of two diodes interposed between the PullSel line and the resistors. The BAV99-Q diodes used in this design are the same employed in the digital position sensor conditioning circuit, from which this design draws inspiration.

The circuit also provides flexibility in adjusting the filtering of the input signal. By default, the signal is filtered by an RC network with a cutoff frequency of 48 kHz. For enhanced filtering, especially when acquiring analog signals, an additional capacitor can be placed in parallel with the existing one. The "FilterSel" signal, connected to a shift register output, controls the operation of a MOSFET (NX3008BKS). When the "FilterSel" signal activates the MOSFET, the extra capacitor is connected between the signal line and ground, thereby increasing the low-pass filtering effect. Conversely, when the MOSFET is off, the capacitor remains disconnected, leaving the input signal unaffected by the additional capacitor.

The MOSFET is necessary due to the limitations of the SN74LV595A-Q1 shift register. While it can place its outputs in a high-impedance (Z) state, this feature applies to all outputs simultaneously, preventing selective control of individual outputs. As a result, in normal operation, the shift register's outputs behave as totem-pole (push-pull) logic, meaning each output can only switch between high or low states. For proper operation of the configurable filter, it is essential to leave the capacitor floating when not used, which requires a high-impedance state. The MOSFET is therefore employed to achieve this functionality.

This circuit topology is particularly effective when a very strong pull-up resistor is required, meaning a low pull-up resistance is necessary. This is the case, for example, when interfacing PT1000 temperature sensors, which are characterized by a nominal resistance value of 1000 Ω at 0 °C, matching the sensor's name. In order to accurately read these sensors, the pull-up resistor must form a voltage divider with the sensor's resistance to achieve a voltage near the midpoint of the ADC's dynamic range. This constraint necessitates very low pull-up resistor values, which introduce several challenges.

First, a small pull-up resistance allows more current to flow, leading to higher power dissipation. Second, in the event of a short to the battery voltage on the sensor input line, the pull-up resistor would be subjected to a much higher voltage drop than it was designed to handle, resulting in an excessive current that could

damage the resistor. Moreover, this current would be drawn from the shift register's output, potentially overloading it and causing failure.

The effectiveness of this circuit lies in the use of diodes to select the pull-up resistance, as they prevent reverse current flow, thereby protecting the circuit from overcurrent events in the case of a short to $V_{batt}$ on the sensor line. This protection allows the use of very small pull-up resistances, enabling proper interfacing with temperature sensors such as PT1000, thus expanding the board's compatibility and application possibilities.

The output of this circuit is connected to a microcontroller pin that can be configured to read either analog or digital signals. This flexibility enables the circuit to interface with a wide range of sensors and signal types, making it highly adaptable for different applications.

To support a wide range of different sensors and drivers, different pull-up resistor values are implemented in various instances of this circuit on the board. Since the pull-up resistor is connected through a diode (which introduces an unknown voltage drop), an additional line is used to monitor the voltage between the pull-up resistor and the diode to ensure accurate and reliable measurements. This line is RC-filtered with a cutoff frequency of 159 Hz and connected to an analog input of the microcontroller.

The total number of signals involved in this circuit, excluding the input signal, is four: two signals are used for selecting the desired behavior of the conditioning circuit (pull-up/pull-down selection and filter activation) driven by the shift register, and two signals are needed by the microcontroller to read the conditioned input and the voltage on the pull-up resistor for accurate measurements.

Although measuring the voltage across the pull-up resistor adds complexity to both the circuit design and the microcontroller's sampling algorithm, this approach enables compatibility with sensors that require very low pull-up resistance values, thereby significantly enhancing the board's flexibility and expanding its range of applications.

## 7.3 Pull-Select From MCU

A more efficient solution in terms of required signals is the following:

In this topology, the pull-up or pull-down configuration is controlled directly by the microcontroller. A 3.9 kΩ resistor is placed in series with the "PullSel" line. When the microcontroller pin is configured as an output, it introduces a small series resistance $(55 \pm 25)\Omega$, which is negligible compared to the already present series resistor. Depending on whether the microcontroller output is set to high or low, a strong pull-up or pull-down is achieved.

Additionally, a weak pull configuration can also be realized. When the microcontroller pin is configured as an input, it internally connects the line to a pull-up

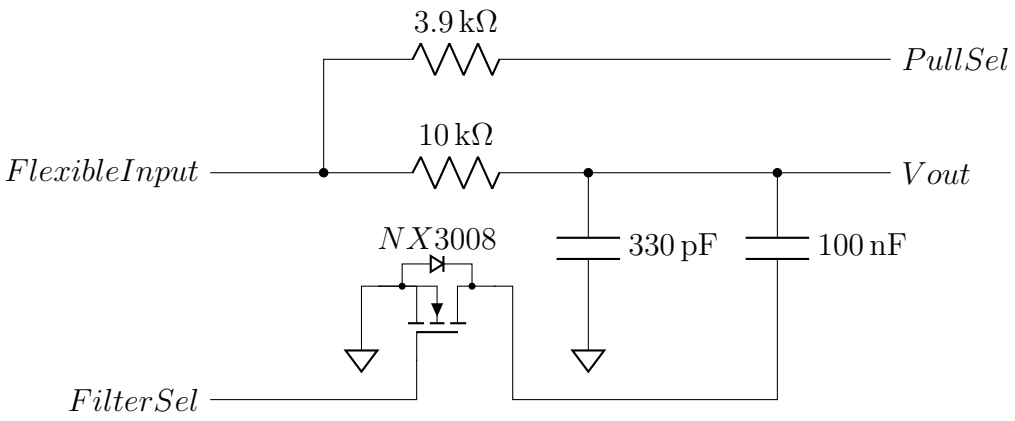


Figure 32: *Circuit diagram showing the flexible input "Pull-Select from Micro"*

or pull-down resistor, depending on the selected setting. The pull-up resistor in CMOS/Automotive logic level typically ranges between 30 kΩ and 42 kΩ, while the pull-down resistor ranges from 43 kΩ to 58 kΩ. Combined with the series resistor already present on the line, this configuration acts as a weak pull-up or pull-down, depending on the desired setting, thus enabling flexible control of the circuit's behavior.

Additionally, this configuration eliminates the need for a diode in series with the pull-up resistor, thereby removing the requirement for an extra signal to read the pull-up voltage. This reduces the total number of signals compared to the previous design, making it more efficient.

The limitation of this design is its inability to use pull-up resistors with very low resistance values, as there is no diode to prevent reverse current flow in the event of a short to $V_{batt}$. To address this, the series resistor has been selected with sufficiently high resistance values to ensure that the current remains within the microcontroller's maximum allowable specifications in the event of a short to $V_{batt}$, providing protection against overcurrent conditions.

Like the earlier design, this circuit allows the filtering of the input signal to be adjusted. The same principle is applied, where an additional capacitor can be connected to modify the filtering behavior, controlled by the "FilterSel" signal.

As before, the output of this circuit is mapped to a microcontroller pin capable of reading both analog and digital signals, maximizing adaptability for different sensor or signal requirements.

This solution is more flexible and does not require additional measurements when used with temperature sensors such as NTC thermistors, as the pull-up voltage is directly provided by the microcontroller and is therefore known.

The series resistance introduced by the microcontroller, when configured in strong pull-up mode, can be accounted for in the measurement. According to the datasheet, the uncertainty of this resistance is $\pm 25\,\Omega$. When applied to the

circuit instance with the smallest implemented pull-up resistor value of 3.9 kΩ, this uncertainty is negligible, contributing to a measurement uncertainty of only 0.63%. Therefore, the impact of this variation in resistance on the overall accuracy of the measurement is minimal.

## 7.4 Single Edge Nibble Transmission

The final design implemented as a flexible input is a modified version of a Single Edge Nibble Transmission (SENT) protocol conditioning circuit.

The SENT protocol, as defined by the SAE J2716 standard [34], is a low-cost and reliable method for digital data transmission in automotive and industrial applications. This protocol is designed to transfer high-resolution sensor data over a unidirectional, point-to-point link, making it particularly suitable for environments where high noise immunity, precision, and minimal wiring complexity are crucial. SENT is ideal for communication between sensors and control units, like the one discussed in this thesis.

SENT transmits data in nibbles, which are 4-bit blocks. Each SENT message frame begins with a synchronization pulse that allows the receiving unit to recalibrate the signal timing and establish a reference point. This synchronization is critical because SENT operates without a continuous clock signal, using the time between falling edges of the signal, referred to as "tick time", to encode information. The synchronization pulse enables the receiver to compensate for any clock variations caused by manufacturing tolerances or environmental conditions, ensuring accurate timing and robust data integrity. This ability to handle clock drift makes SENT a cost-effective alternative to more complex protocols, particularly in point-to-point communication scenarios.

SENT also includes a Cyclic Redundancy Check (CRC) for error detection, which further enhances the integrity of the transmitted data. The CRC is calculated over the entire frame and sent as part of the message, allowing the receiver to verify that the data has not been corrupted during transmission. This feature is particularly valuable in harsh environments, such as automotive systems, where electromagnetic interference (EMI) may degrade signal quality.

Although SENT is not as fast as other protocols like CAN or SPI, with a data rate of up to 40 kbps, it is typically sufficient for many automotive applications where reliability and resolution are prioritized over speed. This trade-off between speed and resolution makes SENT particularly well-suited for sensor applications that require accurate, high-resolution data transmission without the need for ultra-fast updates.

In accordance with protocol specifications, the SENT conditioning circuit requires a weak pull-up resistor and a two-stage low-pass RC filter with specific time constants for each stage. The resulting cutoff frequency of this circuit is relatively

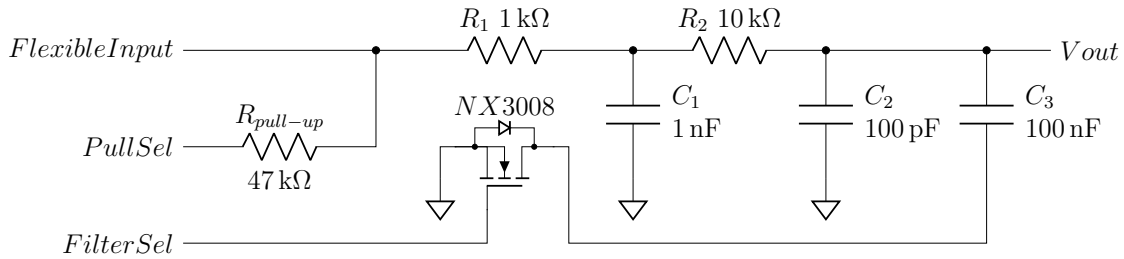


Figure 33: *Circuit diagram showing the flexible input "Sent".*

high, around 100 kHz, as it is designed to process digital signals. The pull-up resistor, according to specifications, should be chosen within a range of 10 kΩ to 55 kΩ, based on system requirements. This is followed by a two-stage RC low-pass filter to attenuate high-frequency noise and enhance signal quality. The first stage comprises $R_1$ and $C_1$, with resistance and capacitance values specified between 448 Ω and 672 Ω, and 1.54 nF and 2.86 nF, respectively, yielding a time constant $\tau_1$ between 0.74 $\mu$s and 1.73 $\mu$s. The second stage consists of $R_2$ and $C_2$, with resistance values required between 4 kΩ and 10 kΩ, and a typical capacitance value for $C_2$ of 47 pF, resulting in a time constant $\tau_2$ between 0.6 $\mu$s and 1.4 $\mu$s.

However, since the SENT-compatible pins on the microcontroller can also be mapped as analog inputs, the circuit was redesigned to accommodate analog signals as well. The pull-up resistor can also be configured as a pull-down resistor using the "PullSel" signal. An additional capacitor can be added in parallel with the second RC filter stage to increase the filtering effect, enabling the circuit to handle analog signals effectively.

The filtering selection is achieved in the same way as in previous designs, using the "FilterSel" signal to enable or disable the extra filtering stage as needed. This allows the circuit to be versatile, handling both SENT digital signals and analog signals with appropriate filtering when required.

The component values implemented in the final design differ slightly from those specified in the protocol datasheet. This adjustment was made to reuse components already present in other sections of the board. The pull-up resistor was selected as 47 kΩ, while the two RC stages were implemented with $R_1 = 1$ kΩ, $C_1 = 1$ nF, $R_2 = 10$ kΩ, and $C_2 = 100$ pF. Consequently, the time constants for both stages are equal at 1 $\mu$s, which, in the case of the first filtering stage, is slightly outside the specified range.

For the design of the first RC stage, $R_1$ was selected with a value slightly higher than the maximum specified in the protocol, and a 1206 package was chosen, unlike the other resistors in the design, which use the smaller 0402 package. This decision was based on experimental observations made during electromagnetic compatibility (EMC) testing. During these tests, high-frequency power signals are injected into the board through the input, causing the first-stage filtering capacitor to behave

like a short to ground. Consequently, a significant current, referred to as bulk current, flows through the $R_1$ resistor. To mitigate potential damage due to the bulk current and to improve power dissipation capabilities, a higher resistance value was selected, and the larger 1206 package was chosen for $R_1$, as it is better suited for handling higher currents and dissipating heat more efficiently than the smaller 0402 package.

# Chapter 8

# Safety Features

Since the primary application of the control board is to manage a dual inverter configuration, it is equipped with two distinct gate driver interfaces, one for each gate driver board. These interfaces handle critical signals necessary for controlling the inverters and ensuring the safe operation of the power electronics. Each interface is paired with safety circuitry, including overcurrent and overvoltage detection, as well as hardware safety logic, which will be discussed in detail in this chapter.

## 8.1 Overcurrent Detection

One of the most critical signals from the gate driver interface is the current feedback for each phase. This signal, which originates from current sensors is ensured to be within the expected voltage range and properly insulated from high voltages by the driver board. It is an analog voltage in the range of 0-5 V. Since the current in the phases can flow in both directions, a value of 2.5 V represents zero current. The range from 0.5 V to 4.5 V is considered linearly proportional to the actual current in the motor phases, while the regions outside this range (0-0.5 V and 4.5-5 V) indicate potential overcurrent conditions, disconnection, or sensor malfunctions.

The microcontroller samples the current at each PWM cycle. Sampling is timed to occur during the middle of the high portion of the PWM signal. This timing is crucial for accuracy and is achieved using the microcontroller's Generic Timer Module (GTM). The GTM allows the ADC to be triggered directly by the same timer responsible for generating the PWM signal, ensuring precise synchronization between PWM modulation and current acquisition.

At a PWM frequency of 20 kHz (a typical frequency for traction inverters), the current is sampled every 50 $\mu$s. While this is fast, it is not always sufficient to ensure a high level of safety in the event of an overcurrent. To achieve better safety, an additional hardware overcurrent detection circuit is implemented to provide instantaneous protection, beyond what is possible with the regular sampling of the

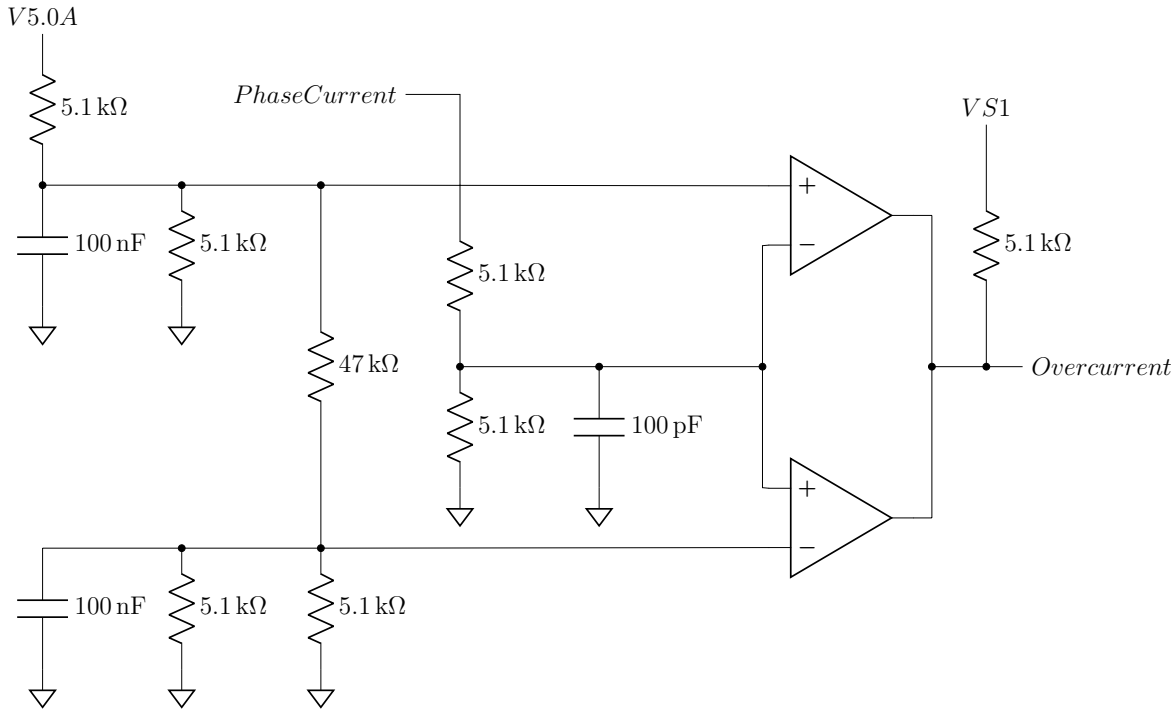


Figure 34: *Circuit diagram showing the adopted solution for the overcurrent detection.*

microcontroller.

The overcurrent detection circuit uses comparators to monitor the current signal and to detect when it exceeds predefined thresholds. When an overcurrent event occurs, a latch stores the event, allowing the microcontroller to respond.

The comparators used are LM2901DT. In the configuration used for the overcurrent detection, they do not include any hysteresis. For this reason, the thresholds are set at 4.75 V and 0.25 V, allowing noise margins to prevent false triggers. Due to their limited common-mode input voltage range (Vcc-2 V), a level shifter circuit is required to ensure the input signals remain within the comparator's operational range. The current signal is scaled using a resistive voltage divider (two equal 5.1 kΩ resistors) to halve its amplitude, ensuring reliable comparator operation. Similarly, the overcurrent thresholds are scaled accordingly to 2.375 V for the upper threshold and 0.125 V for the lower threshold. They are derived from a resistive voltage divider based on the V5.0A supply to keep them as stable as possible.

The LM2901DT comparators have open-drain outputs, meaning they require pull-up resistors to bring their output high. This characteristic allows the outputs of multiple comparators (for both upper and lower current limits) to be connected in parallel. The combined output of these comparators is fed into the latch, ensuring that the latch is triggered if any of the comparators detect an overcurrent condition.

## 8.2 Latch

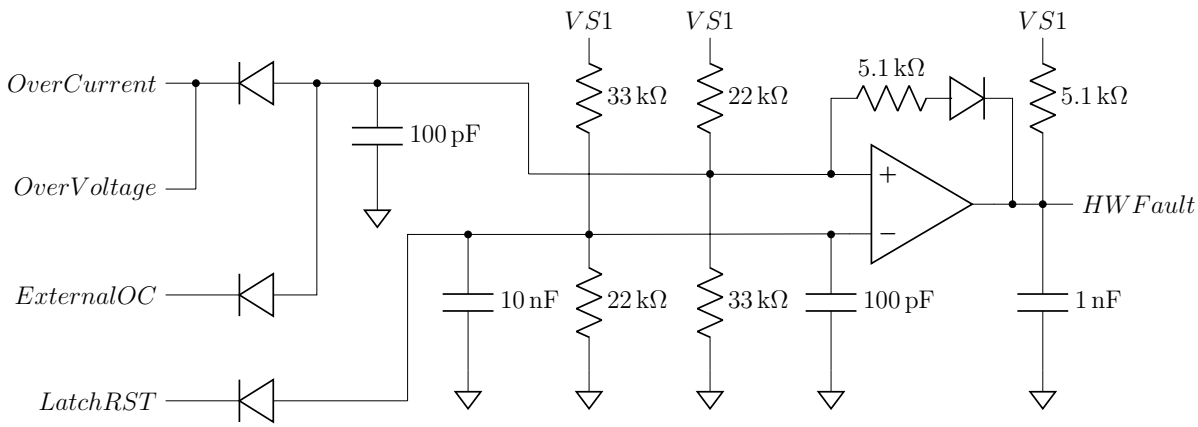


Figure 35: *Circuit diagram showing the adopted solution for the latch using a comparator with a diode on the feedback.*

The latch circuit is particularly critical because overcurrent events can occur within a very limited instant of time. The latch implemented in this design consists of a comparator with a diode in the feedback loop, ensuring that once an overcurrent event is triggered, it remains latched until the microcontroller explicitly resets it. This approach guarantees that transient overcurrent conditions are reliably captured and addressed, preventing potential damage to the system.

To further enhance the system's flexibility, the circuit incorporates an OR configuration using diodes, which allows an external overcurrent signal (if present, generated by the gate driver board) to trigger the same latch. This ensures that the latch will respond consistently, regardless of whether the overcurrent event is detected by the external gate driver or by the onboard protection circuit.

The microcontroller can reset the latch via a dedicated reset signal. A diode is placed in series with this reset signal, ensuring that the reset pin from the microcontroller operates in open-drain mode, which is necessary for the correct operation of the latch. Even though the pin from the AURIX™microcontroller connected to this reset line is three-state, the use of the diode ensures compatibility with this setup.

The design of the latch circuit is an adaptation of I&M's existing expertise in using a comparator-based latch configuration. The primary focus of this work was to adjust the design to match the resistor and capacitor values already used in other circuits on the board, thereby minimizing the bill of materials (BOM). This optimization ensures that the design remains efficient while leveraging existing components to reduce costs and simplify production without compromising performance.

## 8.3 Overvoltage Detection

In addition to the overcurrent detection, the board also includes an overvoltage detection system. Since the LM2901DT package includes four comparators, and only seven comparators are needed for the overcurrent detection and latch functions, one comparator remains available. This unused comparator is exploited to monitor the DC-Link voltage for overvoltage events.

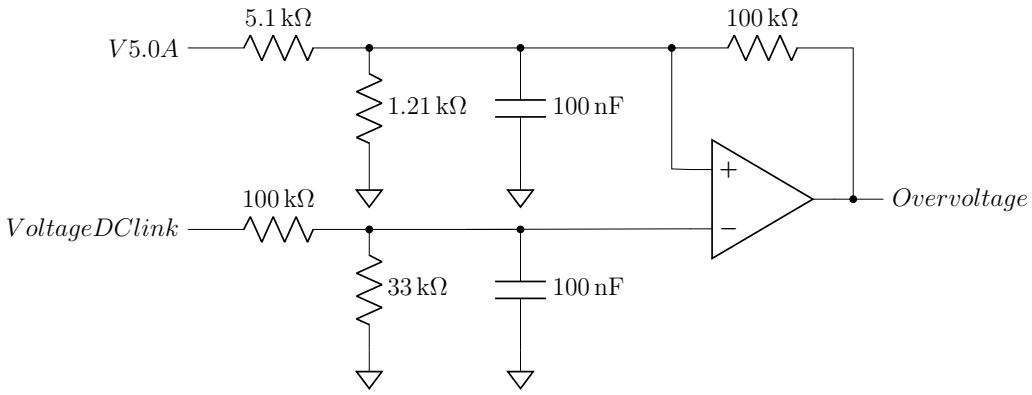


Figure 36: *Circuit diagram showing the adopted solution for the Overvoltage detection.*

DC-Link overvoltage detection is critical because, during regenerative braking, the voltage on the DC-Link can rise above safe operating limits, potentially damaging both the battery and the inverter. Additionally, overvoltage conditions can occur during fault scenarios, such as when the system shuts off the power switches to protect the inverter and motor. In these situations, the energy stored in the stator inductance, which was previously driving the motor, is fed back into the DC-Link capacitor via the freewheeling diodes. This can cause the capacitor to charge to higher voltages, further increasing the risk of damage. Proper overvoltage detection helps mitigate these risks, ensuring safe operation and preventing component failure [35].

To prevent false triggering of the overvoltage detection circuit, the input voltage to the comparator is heavily filtered compared to the overcurrent detection circuit. This is to avoid potential voltage spikes to set the overvoltage signal. Additionally, the overvoltage detection circuit uses a comparator configured with hysteresis to enhance its robustness. The hysteresis prevents minor fluctuations or noise from causing oscillations around the threshold, ensuring that the detection mechanism only triggers when the DC-Link voltage has definitely crossed the critical limit.

To provide adaptability in the system design, the overvoltage detection circuit allows flexible implementation. This means the overvoltage signal can either trigger the latch (similar to the overcurrent detection) or simply be read by the microcontroller without latching. The choice of configuration can be made during the PCB

design phase by selecting the appropriate components to mount, offering flexibility for different applications.

The DC-Link voltage feedback from the gate driver interface is designed to remain within the 0-5 V range, with a linear relationship to the actual DC-Link voltage up to 4 V. Beyond 4 V, the signal enters a non-linear range, where voltages between 4 V and 5 V indicate an overvoltage condition. The thresholds for overvoltage detection are set at 4 V (upper limit) and 3.8 V (lower limit).

To avoid common-mode voltage issues, both the DC-Link voltage and the comparator thresholds are scaled by a factor of 1/4. This means the comparator thresholds are set at 1 V and 0.95 V.

To properly scale the DC-Link voltage for the comparator, a resistive voltage divider consisting of 100 kΩ and 33 kΩ resistors is used, reducing the voltage by a factor of 1/4. Designing the resistors that determine the exact threshold values involves more complex calculations. In the following, the mathematical derivation for designing an inverting comparator with hysteresis is provided.

As previously mentioned, the comparators used in the design have open-drain outputs; however, this is not relevant for the threshold design. The only critical parameters are the output voltage levels, $V_{OL}$ and $V_{OH}$. When the output is low, the comparator pulls the output to ground, resulting in $V_{OL} = 0$ V. When the output is high, the pull-up resistor raises the line to 5 V, giving $V_{OH} = 5$ V. Additionally, the thresholds are derived from the $V_{5.0A}$ voltage, as in the overcurrent protection circuit, to ensure maximum stability. Consequently, the supply voltage $V_{AL}$, from which the reference voltage $V_{REF}$ is derived, in the design is set to 5 V.

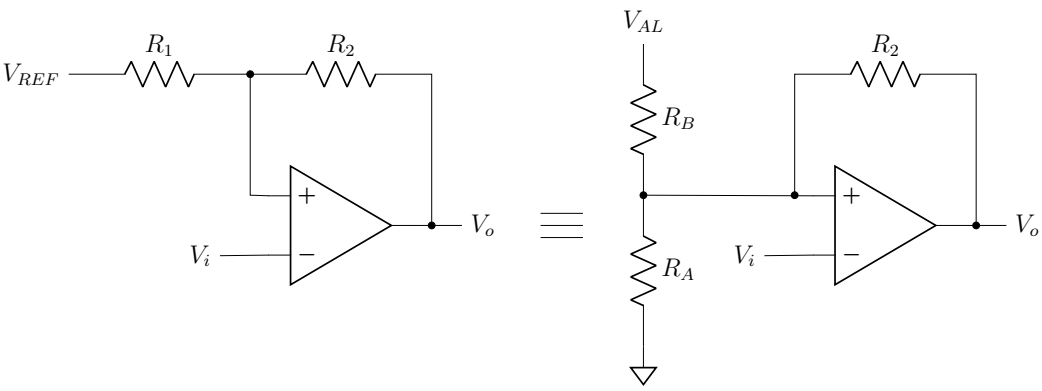


Figure 37: *Inverting comparator with hysteresis.*

Given the following data:

$$V_{AL} = 5 \text{ V}; \quad V_{OL} = 0 \text{ V}; \quad V_{OH} = 5 \text{ V}; \quad V_{TH1} = 1 \text{ V}; \quad V_{TH2} = 0.95 \text{ V}$$

The thresholds characteristic equations of an inverting comparator with hysteresis are:

$$\text{Threshold Mean Value:} \quad \frac{V_{TH1}+V_{TH2}}{2} = \frac{1}{2}(V_{OH}+V_{OL})\frac{R_1}{R_1+R_2} + V_{REF}\frac{R_2}{R_1+R_2}$$

$$\text{Threshold Amplitude:} \quad V_{TH1}-V_{TH2} = (V_{OH}-V_{OL})\frac{R_1}{R_1+R_2}$$

From the amplitude equation:

$$\frac{R_2}{R_1} = \frac{V_{OH}-V_{OL}}{V_{TH1}-V_{TH2}} - 1 = 99$$

Substituting into the mean value equation:

$$V_{REF} = \frac{R_1+R_2}{R_2}\cdot\frac{V_{TH1}+V_{TH2}}{2} - \frac{V_{OH}+V_{OL}}{2}\cdot\frac{R_1}{R_2} = 959.6 \text{ mV}$$

$V_{REF}$ is derived from $V_{Al}$ via the following equation:

$$V_{REF} = V_{AL}\cdot\frac{R_A}{R_A+R_B}$$

from which we get:

$$\frac{R_B}{R_A} = 4.21 \quad \Rightarrow \quad R_B = 5.1 \text{ k}\Omega, \quad R_A = 1.21 \text{ k}\Omega$$

Finally:

$$R_1 = \frac{R_A R_B}{R_A+R_B} = 977.97\ \Omega \approx 1 \text{ k}\Omega$$
$$R_2 = 99\cdot R_1 = 99 \text{ k}\Omega \approx 100 \text{ k}\Omega$$

This design successfully achieves the desired circuit behavior with the intended threshold values. Later in this chapter, simulations of this circuit will be conducted to validate and demonstrate its performance.

## 8.4 Hardware Safety Logic

The interface supports two Safe State (SS) signals, enabling four possible configurations to manage system safety during faults. These signals are essential for gate drivers supporting mechanisms such as Active Short Circuit (ASC), particularly in PMSM applications. In the event of a fault at high speeds, leaving the switches open can generate strong braking torque and large back-EMF, potentially leading to rear-end collisions and overvoltage breakdowns. ASC mitigates these risks by actively shorting the motor windings, absorbing the back-EMF, and producing zero

braking torque, preventing potential damage that could occur with open-circuited motor windings. However, ASC's main drawback is that it can result in excessive current during the transition to a safe state, necessitating power switches with higher current tolerance, which increases both hardware costs and inverter size [36].

Properly managing these signals ensures that, in the event of a fault, the inverter enters the appropriate safe state based on its operating conditions, thereby reducing the risks associated with fault scenarios and enhancing overall system safety.

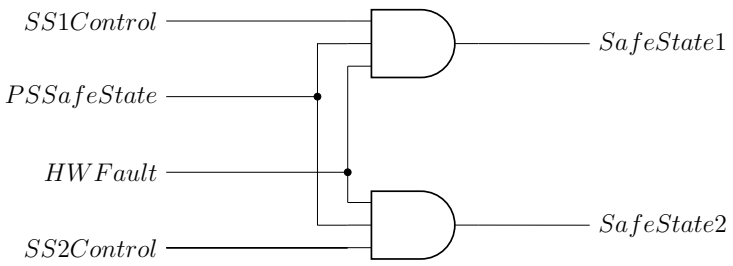


Figure 38: *Circuit diagram showing the adopted solution for the hardware safety logic.*

To meet the safety requirements of the system, the Gate Driver Interface includes a dedicated hardware safety logic, which is duplicated for both gate driver connectors. This logic ensures that safe state signals are appropriately generated and managed, providing a fail-safe mechanism for the inverter control system.

The safety logic is implemented using two three-input AND gates, configured with negated (active-low) logic. Each gate is responsible for generating one of the two safe state signals (SS1 and SS2). These signals control the gate driver board's behavior during fault scenarios.

Each AND gate receives three critical inputs:

- **Microcontroller Control:** One input is directly controlled by the microcontroller, allowing the system to decide dynamically which safe state to activate. This flexibility enables the microcontroller to decide the most appropriate safe state to implement based on real-time system conditions, such as vehicle dynamics and actual speed.

- **Power Supply Safe State:** The second input is connected to the power supply's safe state signal. This input is vital for ensuring safety even if the microcontroller becomes unresponsive. In the event of a microcontroller failure, the external watchdog timeout and the PMIC take control, forcing the system into the default "00" safe state. This prevents potentially hazardous conditions by stopping the inverter and protecting the system from further damage.

- **Hardware Protection Latch Output:** The third input comes from the output of the latch in the hardware protection circuit. If an overcurrent or

overvoltage fault is detected, the latch stores the event, and this signal is used to drive the default safe state "00". By feeding this signal into the AND gate, the system ensures that critical hardware-level faults can immediately trigger a transition to a safe state.

The combination of these three inputs allows for a robust and flexible safe state mechanism. The microcontroller, when functioning correctly, has the ability to make decisions about which safe state is appropriate for the current operating condition. However, if the microcontroller becomes unresponsive, either the power supply or the hardware protection circuit can take over and force the system into a default safe state to prevent damage or unsafe conditions.

In addition to generating the safe state signals (SS1 and SS2) that are sent to the gate driver boards, these signals are also fed back to the microcontroller for monitoring purposes. This feedback mechanism is implemented via 100kΩ series resistors, which decouple the actual safe state signals from the microcontroller inputs. The resistors ensure that the microcontroller can monitor the state of the system without directly interfering with the signals sent to the gate driver boards.

This decoupling provides an extra layer of safety. In the unlikely event of a microcontroller pin failure, the resistors prevent the microcontroller from pulling the safe state lines into an unknown or undesired state, thus maintaining system integrity. By rereading the signals, the microcontroller can confirm that the correct safe states are being implemented and detect potential failures.

## 8.5 Simulations

To validate the functionality of the hardware protection circuit, which encompasses the overcurrent, overvoltage, and latch sub-circuits, and to evaluate its response time, simulations were carried out in LTSpice. The LM2901DT comparator model, sourced from STMicroelectronics, was utilized to ensure accurate simulation of the system's behavior [37].

Figure 39 presents the simulation schematic for the overcurrent, overvoltage, and latch circuits in LTSpice.

For the overcurrent circuit, a 1 kHz sinusoidal waveform was used for the current feedback, consistent with the motor's electrical frequency discussed in the position sensors chapters. A transient analysis was performed to validate the working principle of the circuit.

Figure 40 illustrates the simulation results. The following waveforms are observed:

- Red: Sinusoidal current waveform ($V_{\text{CurrentPhase}}$)
- Cyan: Scaled version at the comparator input ($V_{\text{CurrentCompIn}}$)

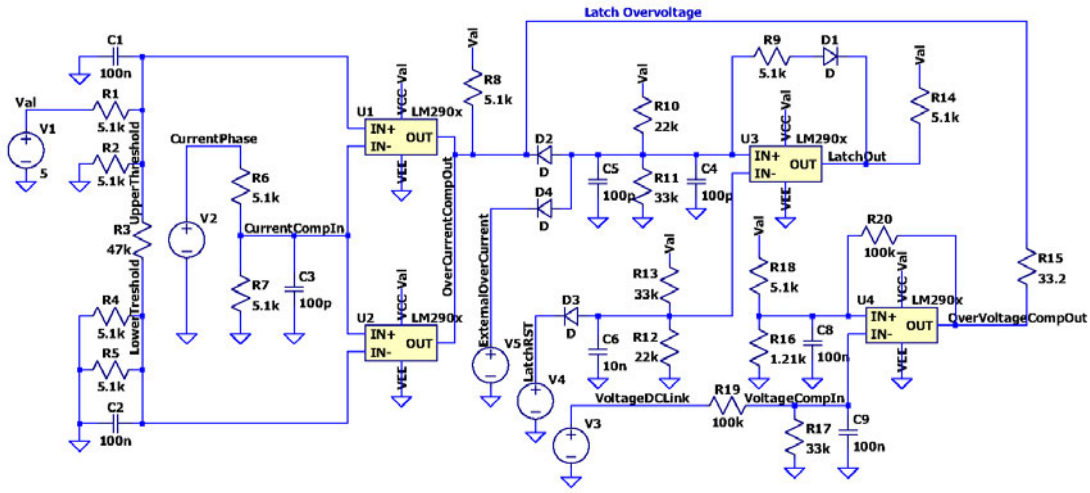


Figure 39: *LTspice scheme of the Overcurrent, Overvoltage, and Latch circuits.*

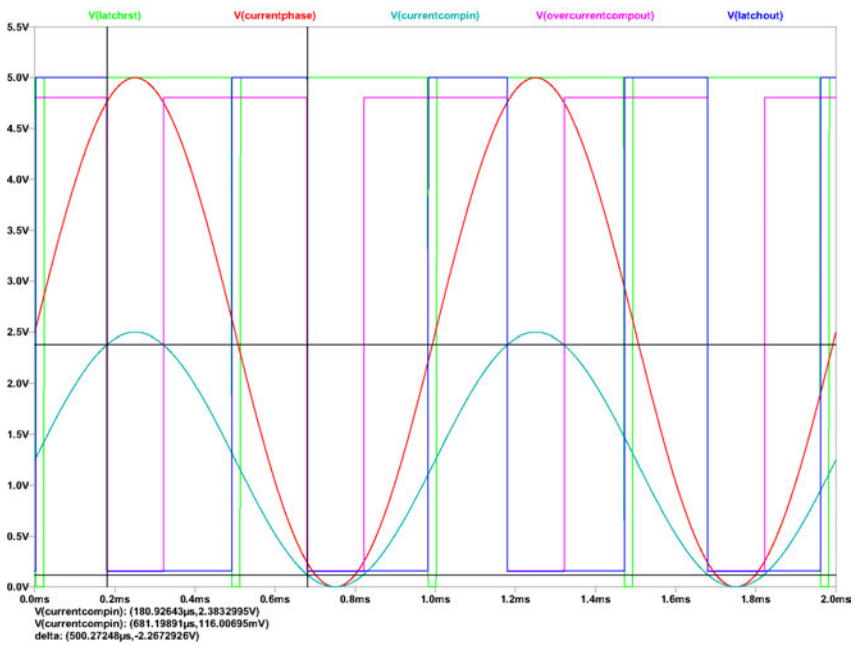


Figure 40: *Time domain simulation results for the overcurrent detection circuit.*

- Purple: Output of the overcurrent comparator ($V_{\text{OvercurrentCompOut}}$)
- Blue: Output of the latch ($V_{\text{LatchOut}}$)
- Green: Latch reset signal ($V_{\text{LatchRst}}$)

The results show that the circuit performs as expected: when the sinusoidal

waveform exceeds the comparator thresholds, the latch output is driven low, triggered by the comparator output. When the current waveform is within the permissible range, the comparator output returns to high, while the latch remains low until a reset signal is applied, which restores the latch to a high state.

The simulation confirmed the overcurrent threshold levels. The upper threshold was measured at 2.38 V, precisely matching the designed value, while the lower threshold was measured at 116 mV, with a deviation of less than 10 mV from the intended design.

A separate transient simulation was performed to verify the correct operation of the overvoltage comparator. A pulsed waveform with a base value of 3 V and an overvoltage value of 5 V was used to simulate the DC-Link voltage. Both "latch" and "non-latch" configurations were tested; the results for the "latch overvoltage" configuration are reported for simplicity.

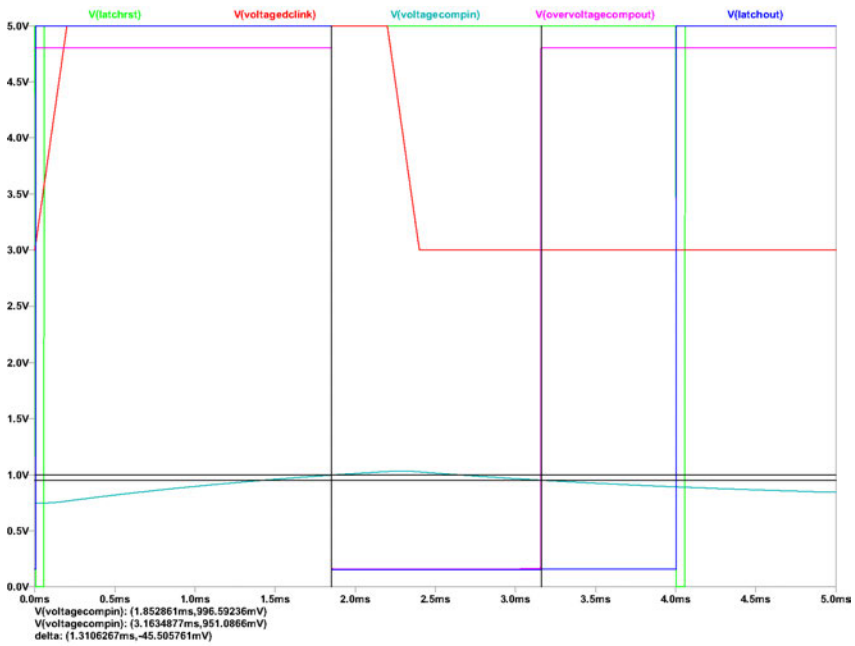


Figure 41: *Time domain simulation results for the overvoltage detection circuit.*

Figure 41 shows the following waveforms:

- Red: DC-Link voltage waveform ($V_{\text{VoltageDCLink}}$)
- Cyan: Scaled and filtered version at the comparator input ($V_{\text{VoltageCompIn}}$)
- Purple: Output of the overvoltage comparator ($V_{\text{OvervoltageCompOut}}$)
- Blue: Output of the latch ($V_{\text{LatchOut}}$)
- Green: Latch reset signal ($V_{\text{LatchRst}}$)

The simulation demonstrates the expected behavior in the "latch overvoltage" configuration. The thresholds measured in the simulation were 996.5 mV for $V_{\mathrm{TH1}}$ and 951.5 mV for $V_{\mathrm{TH2}}$, both very close to the designed values. The comparator output returns high once the input voltage crosses the second threshold, while the latch retains the overvoltage event until a reset signal is applied.

Finally, an evaluation of the response time of the overcurrent circuit was performed using a sawtooth input waveform with a peak-to-peak voltage of 4 V and a DC offset of 3 V. This ensures a trigger of the upper threshold with a sharp edge, avoiding triggering the lower threshold.

The delay between the moment when the current waveform crosses the upper threshold and the latch output goes low was measured at approximately 1.74 $\mu$s. This value will be verified during the testing of the board.

## 8.6 Testing

To evaluate the overcurrent circuit, the upper and lower thresholds were first measured using a multimeter. The measured values were UpTh = 2.372 V and LowTh = 0.122 V, both very close to the designed values, demonstrating the accuracy of the implemented circuit. A signal generator with two outputs was used to generate both the input signal and the latch reset signal. The results of the testing are shown in Figure 42.

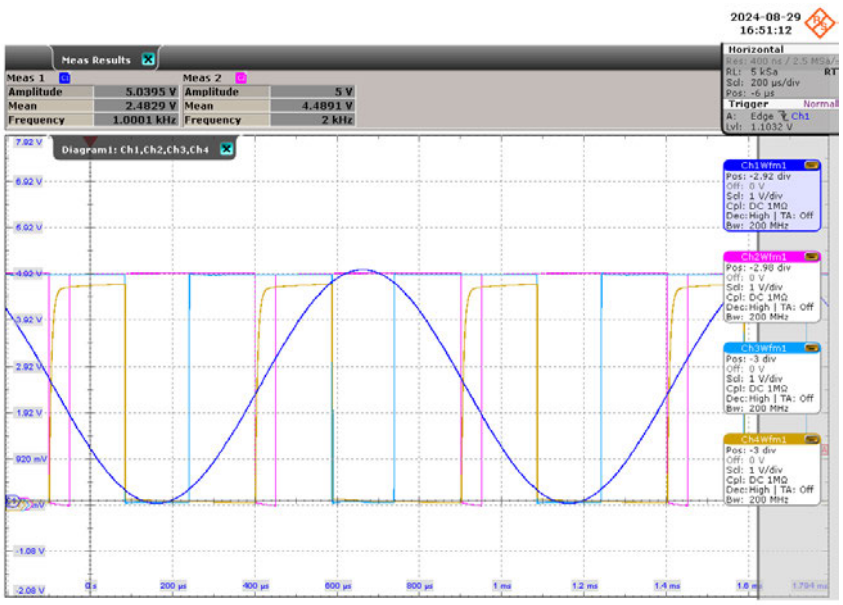


Figure 42: *Oscilloscope capture of the overcurrent detection circuit.*

The oscilloscope output confirmed the desired behavior of the circuit. The

following waveforms are observed:

- Blue: Current waveform.
- Purple: Latch reset signal.
- Light blue: Output of the overcurrent comparator.
- Yellow: Output of the latch.

An additional test was performed to measure the delay between the threshold triggering at the comparator and the corresponding logic level at the latch output. The same test conditions used in the simulations were applied. A sawtooth waveform with a peak-to-peak amplitude of 4 V and a DC offset of 3 V (1 V minimum, 5 V maximum) was generated by the signal generator to trigger only the upper threshold.

The oscilloscope was configured to trigger on the rising edge of the input signal, positioning the 0-time mark at the center of the screen. By zooming in on the time axis, it was possible to measure the actual delay in the real circuit. The oscilloscope's native hold time measurement feature was utilized to quantify the delay, defined as the time between the rising edge of the input signal and the falling edge of the latch output, both measured at 50%. Additionally, the logic output of the hardware safety logic was also captured.

Figure 43 presents the oscilloscope results.

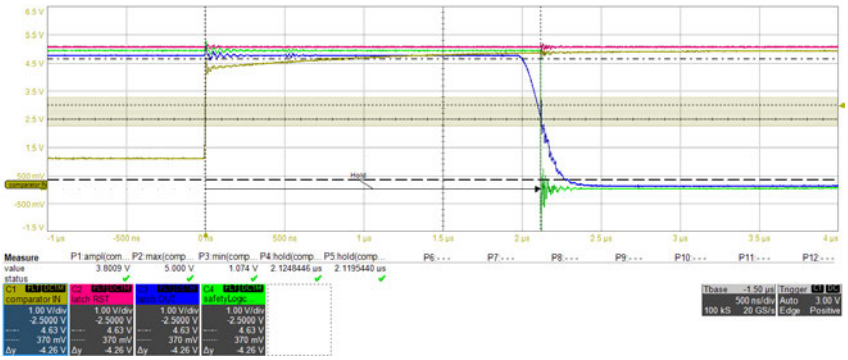


Figure 43: *Overcurrent response delay test results.*

The following waveforms can be observed in the figure:

- Yellow: Input sawtooth signal.
- Pink: Latch reset signal.
- Blue: Latch output.

- Green: Safety logic output.

The results indicate that the actual behavior of the latch output is not as sharp as observed in the simulation. However, this slower transition is mitigated by the hardware safety logic sub-circuit that provides a very sharp digital output. This explains why the logic gate was not included in the simulations, as its propagation delay is on the order of nanoseconds and is negligible for the application.

The measured delay in the real circuit was slightly longer than predicted by the simulations but remained within acceptable limits for the intended application. This discrepancy could also be attributed to the signal generator, which, as evident in the oscilloscope screenshot, exhibits non-ideal behavior following the rising edge.

In conclusion, a 2 $\mu$s time interval for overcurrent detection represents a significant improvement compared to the 50 $\mu$s in the previously considered example. This circuit has proven to be an effective solution for preventing damage in an overcurrent scenario.

# Chapter 9

# SPI Level Shifter

The onboard peripherals communicate with the microcontroller primarily via the Serial Peripheral Interface (SPI). The microcontroller is equipped with five independent SPI lines, each designated for different functions. One SPI line is exclusively dedicated to the onboard PMIC, another manages the communication with the Gate Driver Board for Inverter 1, while a third is shared between Inverter 2 and the rest of the onboard peripherals. The remaining two lines are used for SSI communication to handle position sensor data.

The SPI line shared across the board peripherals and the second inverter faces the challenge of communicating with components that operate at different logic levels. Specifically, the gate driver boards operate on 5 V SPI communication, while the accelerometer and memory operate at 3.3 V logic. This mismatch in voltage levels creates the need for a level-shifting circuit to ensure safe and reliable communication between the microcontroller and the 3.3 V peripherals.

The level-shifting mechanism can be implemented by several methods including:

- Resistive voltage dividers
- Active level shifter integrated circuits (ICs)
- MOSFET-based configuration.

While resistive voltage dividers could technically be used to step down the 5 V SPI signals to 3.3 V, this approach presents several challenges. First, voltage dividers do not solve the reverse issue of stepping up the MISO (Master In Slave Out) signal from 3.3 V to 5 V, which, in theory, is required for proper communication with the microcontroller. Second, voltage dividers, in the presence of parasitic capacitance, can behave like low-pass filters. Even with a small input capacitance (such as 10 pF) on the input pins of the 3.3 V peripherals, this can cause signal degradation at higher SPI frequencies (above 1 MHz). This results in the rounding of signal edges, slower transitions, and ultimately leads to unreliable communication

due to the inability to maintain sharp signal transitions necessary for high-speed operation.

Another viable option could have been the integration of ICs that actively translate the logic levels between 5 V and 3.3 V in both directions. However, this solution is not optimal, as it would introduce an additional part number (PN) into the design, increasing both complexity and cost. This would unnecessarily complicate the Bill of Materials (BOM), making the overall design less streamlined without significant performance benefits compared to a MOSFET-based solution.

Given these reasons, the latter configuration was selected for this design. This decision was influenced by a few key factors. First, the specific MOSFET part number used in the design, the NX3008NBKS, was already implemented in other sections of the board, allowing for the reuse of existing components. Second, this MOSFET-based solution provides reliable, fast switching for SPI communication, ensuring the signal integrity necessary for high-speed data transfer without the worries of parasitic capacitance.

## 9.1 MOSFET-Based Level Shifter

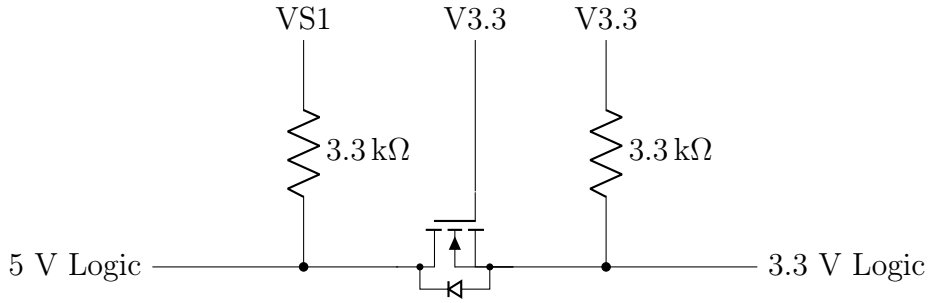


Figure 44: *Circuit diagram showing the adopted solution for the MOSFET-based level shifter.*

What follows is a functional description of a MOSFET-Based Level Shifter operating principle

### From Microcontroller to Peripheral (MOSI, CLK, CS lines)

When the microcontroller is not actively driving the SPI line, both the drain side (connected to the microcontroller) and the source side (connected to the peripheral) are held at a high logic level (5 V on the drain side and 3.3 V on the source side) due to the presence of the pull-up resistors on both sides.

When the microcontroller drives the drain side low, the body diode of the MOSFET starts conducting, progressively lowering the voltage on the source side (connected to the peripheral). As the voltage on the source side drops below a certain

threshold (the $V_{gs}$ threshold of the MOSFET), the MOSFET turns on, and a conductive channel is formed between the drain and source. This effectively pulls the low signal (0 V) from the drain side (microcontroller) to the source side (peripheral), bringing the logic low to the peripheral.

When the microcontroller drives the drain side high again, the MOSFET initially remains on because the conductive channel is still formed. As a result, the high voltage from the drain side (5 V) starts to propagate to the source side. However, once the source voltage rises to a certain point (reaching the MOSFET's $V_{gs}$ threshold), the MOSFET turns off. At this point, the source side remains at a stable high logic level of 3.3 V, maintained by the pull-up resistor on the source side. With the MOSFET no longer conducting, the logic high is reliably held at 3.3 V on the peripheral side, ensuring proper communication.

**From Peripheral to Microcontroller (MISO line)**

For the MISO line in SPI communication, the direction of the signal is from the source side (3.3 V peripheral) to the drain side (5 V microcontroller). Both sides are at high logic levels when idle, held there by the pull-up resistors.

When the peripheral drives the source side low, the $V_{gs}$ of the MOSFET decreases. This causes the MOSFET to turn on, creating a conductive channel between the source and drain. The low logic level from the source side is thus propagated to the drain side, allowing the microcontroller to correctly read a low signal.

When the peripheral drives the source side high (to 3.3 V), the MOSFET initially stays on since the channel is still formed. The 3.3 V signal from the source side is passed to the drain side. However, as the $V_{gs}$ drops to zero, the MOSFET turns off. At this point, the pull-up resistor on the drain side begins pulling the voltage up from 3.3 V to 5 V.

The MOSFET-based level shifter circuit is crucial for adapting logic levels between the microcontroller and 3.3 V peripherals on a shared SPI bus, which also includes 5 V peripherals like the gate drivers. Without it, 5 V signals could reach the 3.3 V components, risking damage or communication errors. Additionally, 3.3 V components could interfere with communication by clamping the high logic level when 5 V is expected. The level shifter effectively decouples the 3.3 V peripherals, ensuring safe and reliable communication across all components on the shared SPI lines.

## 9.2 Simulations

To validate the performance of the level shift circuit, a simulation was conducted. Initially, the voltage divider-based level shifter was simulated to demonstrate its degradation in performance as the frequency increases, particularly beyond 1 MHz. This simulation highlights how the voltage divider struggles to maintain clear

transmission data at higher frequencies, confirming the need for more robust level-shifting techniques in high-speed applications.

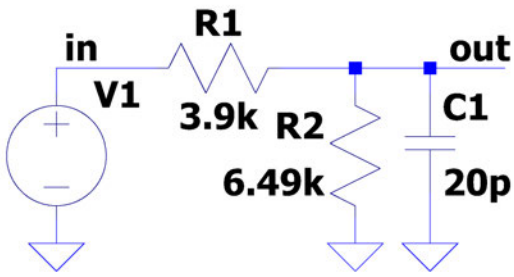


Figure 45: *LTspice scheme of the level shifter based on resistive voltage divider.*

In the simulation of the resistive voltage divider level shifter circuit, a conservative parasitic capacitance of 20 pF was considered to account for both the accelerometer and memory pins. The results, shown in Fig. 46, depict a square wave input signal at three frequencies: 100 kHz, 1 MHz, and 10 MHz. From the simulation, it is evident that while the circuit performs adequately at lower frequencies, it is not suitable for frequencies exceeding 1 MHz. The degradation in performance becomes particularly apparent at 10 MHz, where the output signal is significantly distorted, making evident the limitations of this configuration for high-speed applications.

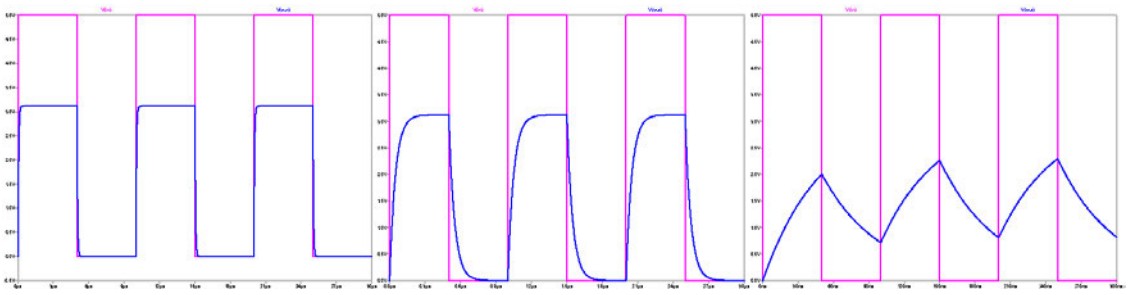

Figure 46: *Time domain simulation results with 100 kHz, 1 MHz, and 10 MHz input frequencies.*

The implemented level shifter circuit, based on a MOSFET, was simulated to validate its performance. The simulation was conducted in both directions to represent both the MOSI and MISO lines in a typical SPI communication. The circuit diagram, as shown in Fig. 47, was implemented in LTSpice, with the MOSFET model for the NX3008NBKS imported from the Nexperia website [38]. Also in this

simulation, a generic parasitic capacitance of 20 pF was considered on the receiver side for both peripherals and microcontroller inputs.

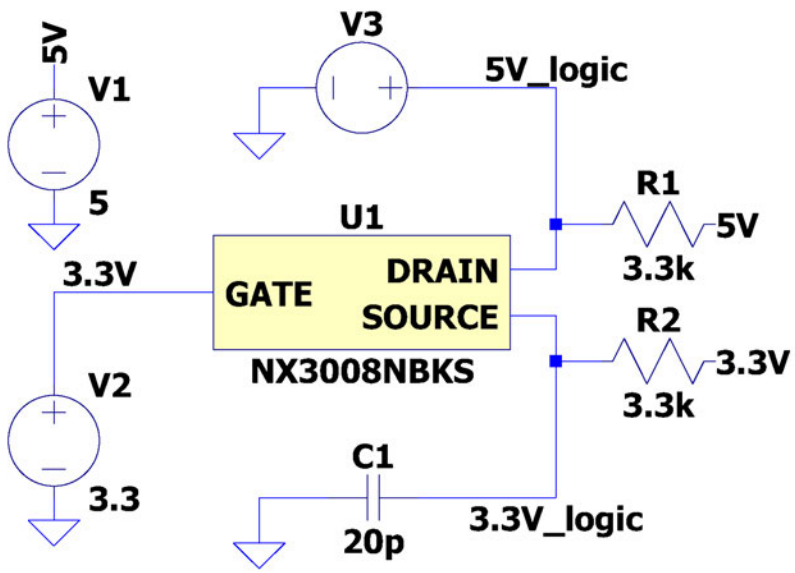


Figure 47: *LTspice scheme of the level shifter based on MOSFET using NX3008NBKS.*

The simulation results illustrate the behavior of the MOSFET-based level shifter at input frequencies of 100 kHz, 1 MHz, and 10 MHz. In Fig. 48, the MOSI line is driven by a 5 V logic signal. Despite the presence of voltage spikes during transitions, the logic levels remain consistent with 3.3 V logic on the source side. An evaluation based on the memory datasheet's input voltage thresholds confirmed that the minimum high voltage level ($V_{IH}$) required is 2.31 V, while the simulation shows that even at 10 MHz, the receiver side voltage remains consistent at 3.3 V, ensuring correct communication between the two logic levels.

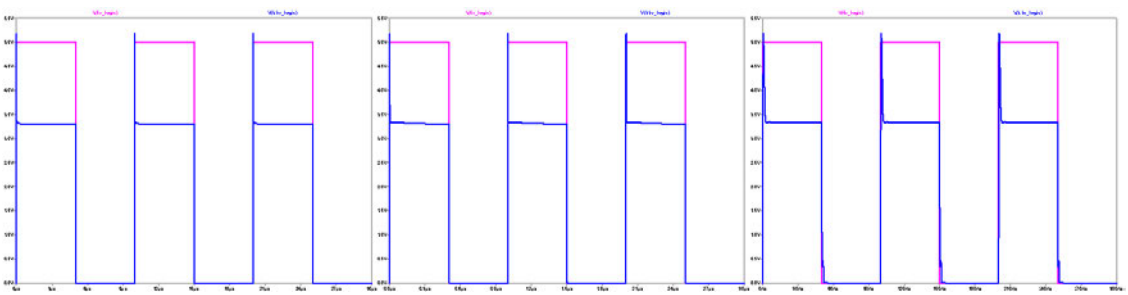

Figure 48: *Time domain simulation results with 100 kHz, 1 MHz, and 10 MHz input frequencies - MOSI line.*

In Fig. 49, the MISO line shows that at higher frequencies, the logic voltage on the drain side becomes clamped at 3.3 V due to the slower response time of the pull-up resistor. This occurs because the pull-up resistor cannot be too small, as reducing its value would lead to excessive power dissipation. However, this is not an issue because the microcontroller can be configured to operate in Transistor Transistor Logic (TTL), where any voltage above 2 V is interpreted as a high signal. Therefore, even though the MISO line is clamped at 3.3 V, the microcontroller still interprets this as a high logic level, maintaining reliable communication at high frequencies.

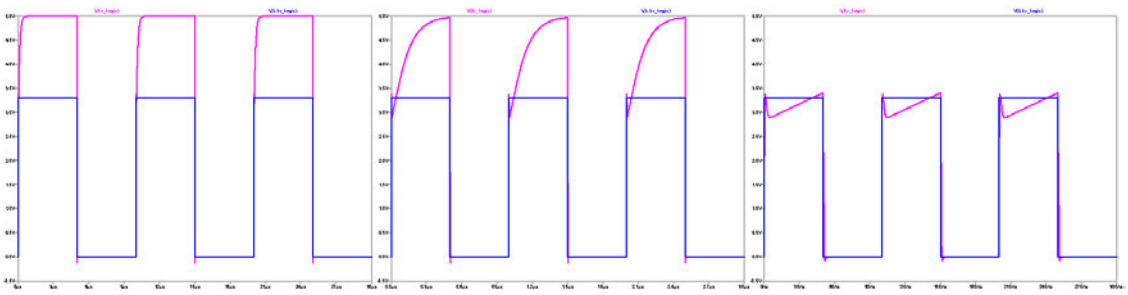

Figure 49: *Time domain simulation results with 100 kHz, 1 MHz, and 10 MHz input frequencies - MISO line.*

# Chapter 10

# PCB Design

Once the schematic design was completed and all signals were correctly connected to the microcontroller, the subsequent steps in the PCB design were carried out by specially trained employees of I&M and monitored in the third person to ensure the best possible results. The first step involved initiating the packager tool, which organizes all components instantiated in the schematic by assigning them unique identifiers. This step is crucial as it generates a comprehensive list of components and their corresponding nets, providing the foundation for the later stages of component placement and PCB layout.

After obtaining the complete list of components, the total space required by the physical footprint of each component was compared to the surface area of the intended PCB. The physical dimensions of the board were constrained by the requirements of the inverter design, where the gate driver and power stage were already finalized prior to the board's design. The resulting percentage of occupied surface area was used to determine the appropriate stackup needed to route all signals effectively. The calculated occupied area was approximately 45%, a relatively high value that typically requires an 8-layer stackup. However, to reduce costs, a 6-layer stackup was selected. If the 6-layer configuration proves insufficient during layout design, it is possible to upgrade to an 8-layer stackup, although downsizing is more challenging, as it would require a complete redesign of the layout.

Another important factor when selecting the stackup is the microcontroller package type, as it typically has the highest number of nets, requiring the most complex routing. The microcontroller chosen for this board uses an LFBGA292 package, which has pad connections distributed across the entire surface. Due to this, even if the board's component-to-surface ratio is low, a stackup with fewer than six layers would not allow for complete routing of the microcontroller pins.

Once the stackup was selected, the Constraint Manager tool within Xpedition Enterprise was utilized to define the physical constraints for the PCB traces. This tool allows for the specification of various parameters, such as the characteristic impedance of certain traces, which is essential for components like the Ethernet

interface that require controlled impedance connections. Additionally, it enables the definition of trace widths for specific nets, such as larger traces where a high current is expected. Another key feature of the tool is the ability to define restricted areas around components, such as the microcontroller, where specific routing rules apply. For example, due to the close proximity of the microcontroller pads, the Constraint Manager allows for the use of thinner traces to ensure all signals are routed properly.

Once these steps are addressed, the layout work begins. Initially, components required for specific functions are grouped together to facilitate routing. For example, components forming circuits such as hardware protection are aggregated into blocks. These blocks are then distributed and rotated on the board surface to optimize routing. Components like anti-reverse diodes and the board's power supply are placed near the external power connector to minimize the length of the power traces. Where possible, particularly for components prone to heat generation, vias are placed underneath to channel heat from the top to the bottom of the board.

In general, both the top and bottom layers are used for component placement and do not follow strict net routing rules due to the forced transitions imposed by the components. Layers 2 and 5 are typically designated for the ground plane and power plane, respectively. The central layers (3 and 4) are usually used for signal routing, one for vertical and the other for horizontal traces, except in the area around the microcontroller, where additional constraints are imposed by the complexity of its pin configuration.

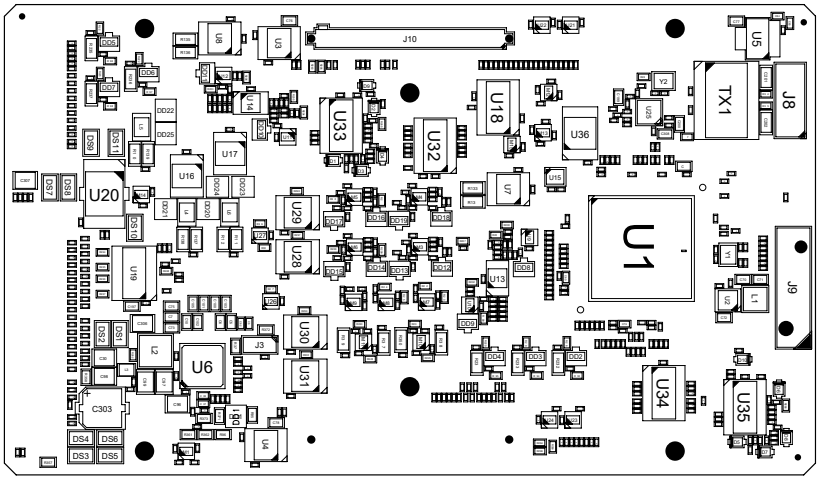


Figure 50: *Control board top layer placement*

# Chapter 11

# Conclusions

This thesis has contributed to the European HiEFFICIENT project, which aims to advance powertrain inverter design by improving energy efficiency, reducing costs, and promoting the adoption of electric mobility and green energy systems. Specifically focused on the control board, this work aimed to develop a flexible, modular, and safety-oriented solution to meet the stringent demands of modern electric vehicle powertrains.

The control board prototype presented in this thesis successfully demonstrates a modular and adaptable architecture, capable of supporting multiple inverter topologies and diverse powertrain configurations. Its versatile design allows it to drive both single and dual Voltage Source Inverters as well as 3-level inverters, providing essential scalability for a range of EV applications. This flexibility is particularly beneficial for electric vehicles with multiple motors, where a unified control board can efficiently manage the operation of multiple traction inverters, reducing system complexity, cost, and space requirements. By minimizing the need for additional control hardware, the overall system design is streamlined, enhancing both efficiency and integration.

A key focus of the design was ensuring system safety and reliability. The control board incorporates multiple protection mechanisms, including reverse polarity protection through diodes and external relays, as well as dual power supply compatibility to ensure uninterrupted operation in the event of power source failures. Additionally, hardware fault detection circuits provide a rapid response time of 2 $\mu$s to potential overcurrent and DC-Link overvoltage conditions, effectively preventing system damage. The integration of hardware safety logic further enhances reliability during fault conditions by allowing the inverter to switch to freewheeling or active short circuit modes, depending on the operational state. This management of safe states external to the microcontroller ensures secure operation, even in the unlikely event of a microcontroller failure, safeguarding the system from critical faults.

The board also incorporates advanced features to enhance adaptability. It supports analog position sensors in both single-ended and differential wiring configurations, utilizing a multiplexer to select between the two modes. Additionally, it interfaces with digital position sensors, including simple latching devices and SSI sensors, using selectable pull-up or pull-down resistors or a full-duplex transceiver, respectively.

The board's ability to handle various communication protocols such as SENT, CAN, and Ethernet ensures robust, high-speed data exchange and system diagnostics, further improving integration into different powertrains.

To enhance the board's adaptability, it integrates programmable analog and digital inputs using shift registers in a daisy-chain configuration, ensuring efficient resource management. This design handles a large number of configuration signals while minimizing microcontroller resource usage, allowing for flexible input programmability. It supports adjustable low-pass filtering characteristics and the selection of pull-up or pull-down resistors, ensuring compatibility with analog, digital (on/off), and frequency signals. Combined with high-side and low-side drivers, this flexibility enables seamless interfacing with a wide range of external systems and devices.

Throughout the development process, simulations were conducted using specific device models sourced from suppliers, including BAV99, LM290, OPA316, and NX3008NBKS, to verify performance and ensure compliance with application requirements. These simulations facilitated the optimization of design choices, such as comparing the voltage divider and MOSFET-based solutions for the level shift circuit, and were crucial in determining the effective cutoff frequency for the low-pass filter in the position sensor conditioning circuits. The insights gained from these simulations allowed the selection of the most suitable designs to be implemented on the board, making simulations an indispensable step in the overall design process.

Tests conducted on the actual components confirmed the intended operation of the circuits, validating the design under real operating conditions. This experimental verification ensured that the theoretical design and simulations translated into practical functionality, reinforcing the board's reliability and compliance with the stringent requirements of automotive standards.

In conclusion, the control board developed in this thesis successfully addresses the key challenges of modularity, safety, and adaptability in traction inverter control systems. By combining theoretical design, simulations, and experimental validation, the resulting board provides a high-performance, versatile solution well-suited to meet the rigorous demands of modern electric vehicle powertrains, contributing to the advancement of energy-efficient, reliable, and scalable electric mobility solutions within the European HiEFFICIENT project.

# Bibliography


[1] [redacted]. Application Note.

[2] [redacted] Application of Low-Resolution Hall Position Sensor in Control and Position Estimation of PMSM—A Review. *Energies*, 17(17):4216, August 2024.

[3] SN65LBC179 | Buy TI Parts | TI.com.

[4] [redacted].

[5] [redacted]. SPI communication protocol, November 2019.

[6] Ideas & Motion, September 2024.

[7] [redacted] | ProfiWeb s.r.o. HiEFFICIENT.

[8] [redacted] Optimisation of current harmonics for three-level VSI based induction motor drive suitable for traction application. *IET Power Electronics*, 11(9):1529–1536, August 2018.

[9] [redacted] Beyond the State of the Art of Electric Vehicles: A Fact-Based Paper of the Current and Prospective Electric Vehicle Technologies. *World Electric Vehicle Journal*, 12(1):20, February 2021.

[10] [redacted]. A review of electric vehicle technology: Architectures, battery technology and its management system, relevant standards, application of artificial intelligence, cyber security, and interoperability challenges. *IET Electrical Systems in Transportation*, 13(2):e12083, June 2023.

[11] [redacted] Benchmark of Rotor Position Sensor Technologies for Application in Automotive Electric Drive Trains. *Electronics*, 9(7):1063, June 2020.

[12] [redacted]. PM motors for hybrid electric vehicles. In *2008 43rd International Universities Power Engineering Conference*, pages 1–5, Padova, September 2008. IEEE.

[13] [redacted]. Automotive Traction Inverters: Current Status and Future Trends. *IEEE Transactions on Vehicular Technology*, 68(4):3337–3350, April 2019.

[14] [redacted] Traction inverters in hybrid electric vehicles. In *2012 IEEE Transportation Electrification Conference and Expo (ITEC)*, pages 1–6, Dearborn, MI, USA, June 2012. IEEE.

[15] [redacted] A Review of Multilevel Inverter Topologies in Electric Vehicles: Current Status and Future Trends. *IEEE Open Journal of Power Electronics*, 2:155–170, 2021.

[16] Current Sensors & Transducers: Accurate Current Sensing | LEM.

[17] Infineon Technologies AG. HybridPACK™ Drive - Infineon Technologies.

[18] Infineon Technologies AG. 32-bit AURIX™ TriCore™ Microcontroller - Infineon Technologies.

[19] Infineon Technologies AG. TLF35584QVVS1 - Infineon Technologies.

[20] Xpedition Enterprise.

[21] Infineon Technologies AG. AURIX™ Development Studio - Infineon Technologies.

[22] MATLAB - Il linguaggio del calcolo tecnico.

[23] LTspice Information Center | Analog Devices.

[24] [redacted]. Evaluation and Modeling of Rotor Position Sensor Characteristics for Electric Traction Motors. pages 2016–01–1065, April 2016.

[25] [redacted]. Investigations of Rotor Shaft Position Sensor Signal Processing in Electric Drive Train Systems. In *2018 IEEE Transportation Electrification Conference and Expo, Asia-Pacific (ITEC Asia-Pacific)*, pages 1–5, Bangkok, Thailand, June 2018. IEEE.

[26] [redacted] Rotor Position Estimation Approaches for Sensorless Control of Permanent Magnet Traction Motor in Electric Vehicles: A Review. *World Electric Vehicle Journal*, 12(1):9, January 2021.

[27] [redacted]. Brushless DC Motor Commutation Using Hall-Effect Sensors. 2019.

[28] [redacted]. Software-Based Resolver-to-Digital Conversion Using a DSP. *IEEE Transactions on Industrial Electronics*, 55(1):371–379, January 2008.

[29] [redacted] An Improved Linearizing Digital Interface for Shaft Angle Sensors with Sine–Cosine Characteristic. *IEEE Transactions on Instrumentation and Measurement*, 69(10):8102–8111, October 2020.

[30] OPA2316-Q1 data sheet, product information and support | TI.com.

[31] BAV99 (High-speed switching diode).

[32] SSI Interface Description, 8027422.

[33] THVD1424: Difference between RS-422 and RS-485 4-wire implementation - Interface forum - Interface - TI E2E support forums, December 2023.

[34] J2716A (WIP) SENT - Single Edge Nibble Transmission for Automotive Applications - SAE International.

[35] [redacted]. Analytical investigation of DC link overvoltages during freewheeling for inverters in EV. In *2016 IEEE Transportation Electrification Conference and Expo (ITEC)*, pages 1–6, Dearborn, MI, USA, June 2016. IEEE.

[36] [redacted]. Suppression of Current Fluctuations and the Brake Torque for PMSM Shutoff in Electric Vehicles. *Mathematical Problems in Engineering*, 2019(1):5026316, January 2019.

[37] LM2901 - Low power quad voltage comparator - STMicroelectronics.

[38] NX3008NBK (30 V, 400 mA N-channel Trench MOSFET).

# Appendix A

# Power Consumption Spreadsheet

| | | | | TLF35584QVVS1 | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Component | Part Number | Quantity | | Vpre (SW1) | V5.0 (QUC) | VS1 (QCO) | V5.0A (QVR) | QT1 | QT2 | EVR33 |
| | | | Nominal Voltage [V] | 6 | 5 | 5 | 5 | 5 | 5 | 3 |
| | | | Nominal Current [mA] | 1500 | 600 | 200 | 150 | 150 | 150 | 60 |
| | | | Used Current (Explicit Loads) [mA] | 0 | 78 | 158 | 49 | 150 | 150 | 40 |
| | | | Used Current (All Loads) [mA] | 1144 | 78 | 158 | 49 | 150 | 150 | 40 |
| | | | Available Current [mA] | 356 | 522 | 42 | 101 | 0 | 0 | 20 |
| | | | Power Dissipation [mW] | 868 | 63 | 127 | 40 | 120 | 120 | |
| | | | Total Power Dissipation [mW] | 1336 | | | | | | |
| MCU VDD through TLF11251 | | 1 | | | | | | | | |
| MCU VDDEXT | | 1 | | | 32 | | | | | |
| MUC EVRSB | | 1 | | | 8.0 | | | | | |
| MCU VFLEX | | 1 | | | | | | | | |
| MCU VDDP3 | | 1 | | | | | | | | 40 |
| MCU VDDM | | 1 | | | | | 48 | | | |
| MCU VAREF1 | | 1 | | | | | 0.20 | | | |
| MCU VAREF2 | | 1 | | | | | 0.20 | | | |
| Accelerometer | LSM6DS3 | 1 | | | | | | | | |
| Opamp SinCos | OPA2316QDGKRQ1 | 2 | | | | 1.0 | | | | |
| Voltage Divider SinCos | | 4 | | | | | 0.12 | | | |
| CAN1 | TJA1043T | 1 | | | | 37 | | | | |
| CAN2-3 | TJA1042BT | 2 | | | | 40 | | | | |
| SSI Transceiver | SN65LBC179QDR | 2 | | | | 7.0 | | | | |
| PHY Ethernet | KSZ8081RNAIA | 1 | | | | | | | | |
| Digital PosSens | | 6 | | | 1 | | | | | |
| Flexible Sent | | 4 | | | | 0.05 | | | | |
| Flexible PT100 | | 2 | | | | 2.2 | | | | |
| Flexible NTC | | 6 | | | | 0.6 | | | | |
| Shift Register | SN74LV595AQPW | 3 | | | | 0.40 | | | | |
| Comparator | LM2901DT | 2 | | | | 2.0 | | | | |
| Comp Threshold | | 1 | | | | | 0.5 | | | |
| Latch input voltage divider | | 2 | | | | 0.09 | | | | |
| Logic Gate AND | 74LVC1G11GW-Q100 | 4 | | | | 0.5 | | | | |
| High Side Driver | BTT6200-4ESA | 1 | | | | | | | | |
| Low Side Driver | TLE9104SH | 1 | | | | 10 | | | | |
| TLF11251LD | | 1 | | | 35 | | | | | |
| Driver board 1 | | 1 | | | | | | | | |
| Driver board 2 | | 1 | | | | | | | | |
| Motor sensor 1 | | 1 | | | | | | 150 | | |
| Motor sensor 2 | | 1 | | | | | | | 150 | |

| | | | | NCV1117ST33T3G | TLF11251LD | TLE4253E | TLE4253E | VBD/VBDAUX |
|---|---|---|---|---|---|---|---|---|
| Component | Part Number | Quantity | | V3.3 | V1.25 | V5.0 (ext track1) | V5.0 (ext track2) | |
| | | | Nominal Voltage [V] | 3 | 1 | 5 | 5 | 14 |
| | | | Nominal Current [mA] | 800 | | 250 | 250 | - |
| | | | Used Current (Explicit Loads) [mA] | 66 | 840 | 100 | 100 | 1720 |
| | | | Used Current (All Loads) [mA] | 66 | 840 | 100 | 100 | |
| | | | Available Current [mA] | 734 | -840 | 150 | 150 | |
| | | | Power Dissipation [mW] | 166 | | 80 | 80 | |
| | | | Total Power Dissipation [mW] | | | | | |
| MCU VDD through TLF11251 | | 1 | | | 840 | | | |
| MCU VDDEXT | | 1 | | | | | | |
| MUC EVRSB | | 1 | | | | | | |
| MCU VFLEX | | 1 | | 18 | | | | |
| MCU VDDP3 | | 1 | | | | | | |
| MCU VDDM | | 1 | | | | | | |
| MCU VAREF1 | | 1 | | | | | | |
| MCU VAREF2 | | 1 | | | | | | |
| Accelerometer | LSM6DS3 | 1 | | 1.3 | | | | |
| Opamp SinCos | OPA2316QDGKRQ1 | 2 | | | | | | |
| Voltage Divider SinCos | | 4 | | | | | | |
| CAN1 | TJA1043T | 1 | | | | | | |
| CAN2-3 | TJA1042BT | 2 | | | | | | |
| SSI Transceiver | SN65LBC179QDR | 2 | | | | | | |
| PHY Ethernet | KSZ8081RNAIA | 1 | | 47 | | | | |
| Digital PosSens | | 6 | | | | | | |
| Flexible Sent | | 4 | | | | | | |
| Flexible PT100 | | 2 | | | | | | |
| Flexible NTC | | 6 | | | | | | |
| Shift Register | SN74LV595AQPW | 3 | | | | | | |
| Comparator | LM2901DT | 2 | | | | | | |
| Comp Threshold | | 1 | | | | | | |
| Latch input voltage divider | | 2 | | | | | | |
| Logic Gate AND | 74LVC1G11GW-Q100 | 4 | | | | | | |
| High Side Driver | BTT6200-4ESA | 1 | | | | | | |
| Low Side Driver | TLE9104SH | 1 | | | | | | |
| TLF11251LD | | 1 | | | | | | |
| Driver board 1 | | 1 | | | | 100 | | 860 |
| Driver board 2 | | 1 | | | | | 100 | 860 |
| Motor sensor 1 | | 1 | | | | | | |
| Motor sensor 2 | | 1 | | | | | | |