EA02-025

FORD
OCTOBER 27, 2003

APPENDIX N
BOOKS 59 OF 61

PART 2 OF 4

3 TEST PROCEDURES AND REQUIREMENTS (cont'd)

3.3 Functional Tests (cont'd)

3.3.6 Extended Accelerated Life Test

This is a continuation of the 6 hour Accelerated Life Test 3.3.5 and is considered consistent with never ending improvement. The outcome of this test is to be used for informational purposes to identify potential product improvements. On termination of Test 3.3.5 and subsequent inspection, this test is to be done. It is the same cycle as Test 3.3.5 and is to be continued until all modules no longer conform to sections 3.3.1,2,3 or a maximum of 24 hours.

3.3.7 Monitored Durability Test

3.3.7.1 Monitored Climatic Environment Tests

The Speed Control assembly must endure the Monitored Climatic Environment Tests as specified in Section 3.4.5.1 through 3.4.5.5, and 3.4.5.8 while undergoing the Monitored Durability Test Cycle. The modules are chamber mounted and shall sustain the temperature/voltage/humidity profiles per Figures 8, 8a, 9, and 9a. Each Speed Control module is run in an open control loop with the durability tester downloading test software into the micro.

3.3.7.2 Monitored 1000 Hour Demonstrated Life Test

The Speed Control assembly must endure the 1000 Hour Demonstrated Life Test as specified in Section 3.4.8 while undergoing the Monitored Durability Test Cycle. The modules are chamber mounted and shall sustain the temperature/voltage profile per Figure 8 and 8a. Each Speed Control module is run in the open control loop with the durability tester downloading test software into the microcontroller's RAM.

3.3.7.3 Monitored Extended Life Test

This is a continuation of the 1000 hour Life Test 3.3.7.2 and is considered consistent with never ending improvement. The outcome of this test is to be used for informational purposes to identify potential product improvements. Begin after termination of Test 3.3.7.2 and subsequent inspection. It is the same cycle as Test 3.3.7.2 and is to be continued until all modules no longer conform to section 3.2 or a maximum of 3000 hours.

3.3.7.4 Monitored Durability Test Cycle

Unless otherwise specified, the Speed Control assembly must comply with section 3.3.1,2,3 after sustaining any of the following durability tests. Under no circumstances shall a Speed Control unit, subjected to any of these durability tests, be shipped for vehicle installation.

The load fixture, mounted external to the test chamber, must provide the spring load function per Figure 6 as well as the lost motion device at the point of servo cable attachment. The fixture also contains a position sensing device providing signals to tester to monitor actuator output position.

3 TEST PROCEDURES AND REQUIREMENTS (cont'd)

3.3 Functional Tests (cont'd)

3.3.7 Monitored Durability Test (cont'd)

3.3.7.4 Monitored Durability Test Cycle (cont'd)

The position sensor input is influenced by three members. They are the load spring, the lost motion device and a 2 position, (WOT and idle), accelerator linkage, which is controlled by the test equipment. The accelerator linkage simulates the accelerator of an actual vehicle installation. The lost motion device prevents any pushing on the cable core wire at the fixture end of the cable.

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The lost motion device and the accelerator member are connected to the position sensor such that either may increase the position sensor input.

The load fixture also contains a mechanical "idle" stop such that a fully released Speed Control module has no load on the cable. This "stop" must be designed as durable as possible because the life cycle includes a hard servo release which will pound against the "stop".

The tester shall be capable of stopping on test fault or continuing with test faults. This should be operator selectable at any time during the test for any combination of test stations.

In addition, should a test be interrupted, the state of the test cycle, including the chamber cycle state and power supply cycle state, should be fully recoverable to the previous drive cycle test segment letter A. Test hours and drive cycles should be tracked and recorded on the basis of individual test stations. Should a module be removed for analysis, the remaining stations can continue test. Later, the module under analysis may be returned to test without loss of test hours accountability.

The durability test cycle is comprised of five segments (A-E) as indicated below. Segment A is the I/O diagnostic segment where the I/O circuitry is verified. Segments B-E are the dithering segments where the motor, clutch & associated electronics are exercised.

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3 TEST PROCEDURES AND REQUIREMENTS (cont'd)

3.3 Functional Tests (cont'd)

3.3.7 Monitored Durability Test (cont'd)

3.3.7.4 Monitored Durability Test Cycle (cont'd)

The test cycles are to be loaded while in Monitor Mode (see Section 3.10) for Families C, D, F, G, M. The test cycles are to be loaded through SCP communication for Family 9.

A. CHECK EACH I/O ONCE AFTER STEPS B,C,D,E - FAMILIES C,D,F,G,M

1) Apply main power and de-activator switch power to the module.

2) Wake the monitor routine and download I/O diagnostic routine into RAM. Refer to Figure 16 for the diagnostic code listing. A JUMP command at the end of the code begins the routine. Once the I/O diagnostic is started, no 2-way RS-232 communication from the durability tester is required.

3) The I/O diagnostic routine will provide a continuous stream of characters (via RS-232) from the module defining the state the microcontroller interprets each input. The stream of characters will include 2 characters. The first character will define which I/O. The second character will define the state of the I/O. For example, AL is defined as input SPEED as LOGIC LOW, AH is defined as input SPEED as LOGIC HIGH. Refer to table 18 for definition of all I/O.

4) The INDICATOR LAMP OUTPUT will be triggered by the state of the BRAKE SWITCH input. If the BRAKE SWITCH input is recognized as an "L", then the INDICATOR LAMP output should be high (lamp OFF). If the BRAKE SWITCH input is recognized as an "H", then the INDICATOR LAMP output should be low (lamp ON).

5) The COMMAND SWITCH character G will be followed be the 2 byte A/D conversion of the COMMAND SWITCH INPUT. The tester must decode this conversion and verify the correct state is recognized. It is important that the tester decode and compare the value after the character G, and not confuse it with one of the other valid characters, since it is possible the converted state could be the ASCII representation of one of the other valid characters.

6) The durability tester reads the continuous stream of characters along with applying commands to verify I/O functionality.

3 TEST PROCEDURES AND REQUIREMENTS (cont'd)

3.3 Functional Tests (cont'd)

3.3.7 Monitored Durability Test (cont'd)

3.3.7.4 Monitored Durability Test Cycle (cont'd)

A The dwell time for this segment is 30 sec. - FAMILY 8 ONLY

1) Initialize each individual module into normal control mode by turning on power and sending the "BRAKE OFF" command over the SCP network.

note: the brake off command and speed message must be sent within 3 seconds of power-up or the module will store a fault in EEPROM.

2) The tester shall transmit to each individual unit a vehicle set speed of 96 Km/h (60 mph or 3000 hex).

3) The tester shall then wait for each unit to echo back this vehicle speed in low resolution form.

4) The unit must respond with the echoed vehicle speed within 2 seconds of the set command to the unit.

B The dwell time for this segment is 240 seconds. - ALL FAMILIES

1) Open the DEACT input at Pin 1-9 (no power applied).

2) Download the dithering diagnostic code into RAM. Refer to Figure 16 for dithering diagnostic code listing.

3) Close the DEACT input (apply power). Verify the actuator output angular position moves to 64 steps for the 10 second period.

4) Verify the actuator dithers ± 12 steps for the remaining 230 seconds.

5) Remove Deactivator power from Pin 1-9. Verify a fast return of the actuator output to closed throttle position within 750 ms.

C. The dwell time for this segment is 240 seconds. - ALL FAMILIES

1) Turn main power off & on for 200 ms.

2) Open the DEACT input at Pin 1-9 (no power applied).

3) Download the dithering diagnostic code into RAM. Refer to Figure 16 for dithering diagnostic code listing.

4) Close the DEACT input (apply power). Verify the actuator output angular position moves to 64 steps for the 10 second period.

3 TEST PROCEDURES AND REQUIREMENTS (cont'd)

3.3 Functional Tests (cont'd)

3.3.7 Monitored Durability Test (cont'd)

3.3.7.4 Monitored Durability Test Cycle (cont'd)

5) Verify the actuator dithers ± 12 steps for the remaining 230 seconds.

6) Remove Deactivator power from Pin 1-9. Verify a fast return of actuator output to the closed throttle position within 750 ms.

D. The dwell time for this segment is 240 seconds. - ALL FAMILIES

1) Turn main power off & on for 200 ms.

2) Open the DEACT input at Pin 1-9 (no power applied).

3) Download the dithering diagnostic code into RAM. Refer to Figure 16 for dithering diagnostic code listing.

4) Close the DEACT input (apply power). Verify the actuator output angular position moves to 134 steps for the 10 second period.

5) Verify the actuator dithers ± 12 steps for the remaining 230 seconds.

6) Remove Deactivator power from Pin 1-9. Verify a fast return of the actuator output to closed throttle position within 750 ms.

E The dwell time for this segment is 240 seconds. - ALL FAMILIES

1) Turn main power off & on for 200 ms.

2) Open the DEACT input at Pin 1-9 (no power applied).

3) Download the dithering diagnostic code into RAM. Refer to Figure 16 for dithering diagnostic code listing.

4) Close the DEACT input (apply power). Verify the actuator output angular position moves to 460 steps for the 10 second period.

5) Verify the actuator dithers ± 12 steps for the remaining 230 seconds.

6) Remove Deactivator power from Pin 1-9. Verify a fast return of the actuator output to closed throttle position within 750 ms.

3 TEST PROCEDURES AND REQUIREMENTS (cont'd)

3.4 Environmental Tests

3.4.1 Acceptance Criteria

Modules must meet requirements of Functional Tests outlined in section 3.3.1, 3.3.2, 3.3.3

SECTION 3.4 - ENVIRONMENTAL TESTS			
TEST NUMBER	REFERENCE SPECIFICATION	MODULE CLASS	TEST
3.4.2 thru 3.4.4	ES-F2AF-1A269-BA Electrical Environment Sections 3.4.2 - 3.4.4 & ES-F2AF-1316-AA	A	
3.4.5.1	ES-F2AF-1A269-BA Section 3.4.5 Climatic Environment	V	3.4.5.1 - LOW TEMPERATURE EXPOSURE T1=-40° C 72 Hour Soak See Figure 8
3.4.5.2		V	3.4.5.2 - LOW TEMPERATURE OPERATION T1=-40° C 72 Hour Soak while Monitored See Figure 8
3.4.5.3		V	3.4.5.3 - HIGH TEMPERATURE EXPOSURE T6=+125° C 72 Hour Soak See Figure 8
3.4.5.4		V	3.4.5.4 - HIGH TEMPERATURE OPERATION T2=+115° C 72 Hour Soak while Monitored See Figure 8
3.4.5.5		V	3.4.5.5 - POWERED THERMAL CYCLE T1=-40° C, T2=+115° C 30 Cycles per Time/Temp. Profile (See Figure 8)
3.4.5.6		V	3.4.5.6 - THERMAL SHOCK RESISTANCE T5=-40° C, T6=+125° C 6 cycles / 2 hour soak @ each temp. >10° C/min.
3.4.5.7		V	3.4.5.7 - THERMAL SHOCK ENDURANCE T5=-40° C, T6=+125° C 1000 cycles / 30 min soak @ each temp. >10° C/min. NOTE: -9D844- ONLY
3.4.5.8		V	3.4.5.8 - HUMIDITY/TEMPERATURE CYCLE 5 cycles per Time/Temp./Humidity Profile See Figure 9

SECTION 3.4 - ENVIRONMENTAL TESTS			
TEST NUMBER	REFERENCE SPECIFICATION	MODULE CLASS	TEST
3.4.5.9.2	ES-F2AF-1A269-BA Section 3.4.5 Climatic Environment	IV	3.4.5.9.2 - WATER/FLUIDS INGRESS CAR WASH SPRAY Install Cable & Seal on Servo before test
3.4.5.9.3	(cont'd)	IV	3.4.5.9.3 - WATER/FLUIDS INGRESS HEAVY SPLASH SHOWER Install Cable & Seal on Servo before test
3.4.5.10		II	3.4.5.10 - DUST
3.4.6.1.1 B	ES-F2AF-1A269-BA Section 3.4.6 Mechanical Environment	II	3.4.6.1.1B - VIBRATION ENDURANCE Method (B)
3.4.6.1.2 B		II	3.4.6.1.2B - VIBRATION OPERATION Method (B)
3.4.6.2		II	3.4.6.2 - AUDIBLE NOISE VIBRATION Method (B)
3.4.6.3.3		IV	3.4.6.3.3 - BENCH DROP
3.4.7.1	ES-F2AF-1A269-BA Section 3.4.7 Chemical Environments	IV	3.4.7.1 - SALT MIST ATMOSPHERE
3.4.7.2		I	3.4.7.2 - CHEMICAL RESISTANCE
3.4.8.1	ES-F2AF-1A269-BA Section 3.4.8 Demonstrated Life	V	3.4.8.1 - HIGH TEMPERATURE ENDURANCE NOTE: -[illegible]- ONLY
3.4.8.3		N/A	3.4.8.3 - MECHANICAL WEAR-OUT

jointly determine which potential changes to the process, materials or material sources would have significant impact on the product's function, performance, durability or appearance. The supplier will describe these conditions in the Control Plan, along with either

(1) the revalidation plan that would be followed in each case, or
(2) a provision to submit an amended Control Plan for approval if any of these process changes are planned.

The Control Plan must include a provision that, for any significant change in processing, AGD-FED and the manufacturing location (internal or supplier) shall jointly determine if FV re-testing is required, and, if so, to what degree, i.e., Full or Mini-FV.

No change to processing may be allowed without prior engineering approval of the process changes and the attendant Control Plan changes.

5 <u>INSTRUCTIONS AND NOTES</u>

5.1 <u>Control Plans</u>

Control Plans address all significant design and process characteristics, which include all ES tests and Control Item characteristics. They describe the process potential studies that will be performed for product validation (including FV tests) and the ongoing product and process evaluation for continuing improvement (including IF tests). They include acceptance criteria, sample sizes, frequencies, data analysis methods and reaction plans.

The Control Plan is developed, and updated as necessary, by the manufacturing source in conjunction with the design responsible Product Engineering Office and other appropriate functions such as SQA. The Control Plan defines the management of the upstream production process and part variables (significant process characteristics) that affect the outcome of the ES tests or other significant design characteristics. The Control Plan also identifies the specific ES tests, with their sample sizes and frequencies, that will be performed in order to:

1. Confirm whether the process is being managed effectively.
2. Further identify significant process characteristics.
3. Evaluate performance of marginal processes.
4. Better anticipate the customer effect of proposed process improvements.

For any part on which ES tests have been specified, the manufacturing source must present the Control Plan and any revisions to the design responsible Product Design Office for approval. This Product Engineering Office has flexibility to honor business relationships with suppliers having proprietary processes.

5 INSTRUCTIONS AND NOTES

5.2 Lot Definition

A lot consists of no more than eight hours of production. When shifts are extended beyond eight hours, the product should be separated into at least two lots to provide the additional inspection required by overtime operations. The size of the lot does not affect the minimum sample size. The audit sample sizes are not to be reduced due to short production runs even though 100 percent inspection results.

5.3 Test Reporting and Record Retention

Recording and record retention shall conform to Ford QS-9000.

5.3.1 Production Validation

All PV samples and the test results and data from Production Validation testing must be submitted in report form to ED-PED prior to ISR. Product Engineering Office shall have final authority to approve PV testing.

5.3.2 In-Process

The IP test variable data produced as a result of performing the sample lot test requirements outlined in Section II must be collected and stored for ED-SQA review.

5.3.3 Test Report Contents

Equipment serial numbers, most recent date of calibration and test sample serial number must be recorded on all data sheets Test summaries must be sorted by test temperatures -40°C, 25°C or 125°C, and contain:

1) Sample Size
2) X - BAR
3) High Reading
4) Low Reading
5) Standard Deviation
6) Cp and Cpk
7) Upper Test Limit
8) Lower Test Limit

The records must be stored such that all parametric data for any one sample piece may be recalled with traceability to the lot in which the sample was taken.

5.3.4 Reporting Frequency

Once a month a summary of the reject rates for incoming inspection, line fallout, repair stations, final test and audit tests, separated by part numbers and suppliers, shall be transmitted to ACD-CEMO and STA.

5 INSTRUCTIONS AND NOTES

5.4 Test Correlation

Equipment calibration must be demonstrated at the beginning and middle of each shift by the supplier. Also, test equipment correlation between on-line and audit test equipment shall be performed by supplier. The procedure must be approved by ACD-CEMO and documented in the supplier control document.

5.5 Fallout Analysis

5.5.1 In-Line Fallout

The assembly supplier is required to analyze all in-line fallout at the module level. All components from "isolated case" fallout and a sufficient quantity of "pattern" fallout must be analyzed to determine the root cause. All test methods and data used to identify the root cause will be submitted together with a report in an East-West 8D format. Summary data of these results must be provided to ACD-CEMO monthly.

5.5.2 Returns - Body & Assembly Division/Field

The supplier shall have the capability to analyze all returns and shall identify the root cause of the returns. A report for each identified root cause is to be delivered to ED-PMD on a timely basis. All test methods and data used to identify the root cause will be submitted together with a report in an 8D format. Summary data of these results must be provided to ACD-CEMO monthly.

5.6 Traceability

The manufacturer shall institute a traceability program per Ford Q-101 3.1A for all components:

Electronic Servo Assembly, Electronic Amplifier Assembly, Mechanical Actuator Assembly, Screws and Brackets.

In addition, each time a module is subjected to any of the daily IP indicated in Figure 1, the test number, test results, (parametric data), and date tested shall be traceable from the clearly marked bar coded module serial number. The module serial number shall be contained in the bar code permanently marked on the module housing.

5.7 Repairs

5.7.1 Definition

A repair is defined as the rework required for a module to pass a test requirement. The following restrictions apply.

- A module may be repaired no more than a total of 2 times.
- Any component which has been replaced during rework must be marked for visual identification.

5 INSTRUCTIONS AND NOTES

5.7 Repairs (cont'd)

5.7.2 Procedure

Repair of the modules may not be done until the manufacturers repair procedure is approved by ACD-CEMD.

The repair procedure must:

a. Identify the test station and report weekly results to the manufacturing responsible engineer and be available to ED-FEO on request.
b. Define how the repair is to be performed for each component at each station reporting.
c. Define an acceptance standard to verify the repair was done to the proper component on the proper module.
d. Provide a method of identification and retrieval of the defective component part.
e. Identify the responsible party for investigating the defective component.

5.8 Packaging and shipping

The packaging and shipment of parts must conform to the packaging and shipping guide, latest revision, as defined by the Material Handling Engineering Department, Manufacturing Engineering Office. The packaging must also be approved by ACD-CEMD before PSW.

5.9 Other Engineering PSW Requirements

This section should be understood as an engineering requirement controlled by ACD-CEMD.

1. Equipment list for: FV, Lot Testing and IP Test Stations.

2. All procedures (ie., calibration, maintenance, equipment set up, station aids etc.) must be completed for production and IP test stations. The above procedures must be on display at all times or as specified by ACD-CEMD.

3. An EOL tester handler must default to rejecting assemblies. The method must be approved by ACD-CEMD.

4. The PSW pilot run must be performed with the same methods and control documents and quality inspection as during production. ACD-CEMD must be informed of the pilot run one week prior and be allowed to observe.

5. The supplier must establish a key yield point weekly report form and submit the report to ED-FEO monthly or as requested.

5 INSTRUCTIONS AND NOTES

5.10 SYSTEM MONITOR OPERATION - FAMILIES C, D, F, G, H

5.10.1 General

The system monitor is utilized by the functional In-Process testers and Accelerated Life Testers for communication with the amplifier microcontroller. The communication is RS-232.

5.10.2 Format and Configuration

The system monitor uses a asynchronous serial communication interface in the microcontroller. Figure 3 illustrates the diagram of the system interface. For BASE SPEED CONTROL MODULES, the RECEIVE DATA (RDI) line shares the Speed Signal input pin (J1-3) and the TRANSMIT DATA OUT (TDO) line shares the Transmission Interface output pin (J1-2). For DIAGNOSTIC SPEED CONTROL MODULES, the RECEIVE DATA (RDI) line shares the Brake input pin (J1-4) and the TRANSMIT DATA OUT (TDO) line shares the Transmission Interface output pin (J1-2). The communication has the following format:

- A character has 1 start bit, 8 data bits, 1 stop bit, no parity.
- All characters are in uppercase ASCII format.
- Data is transmitted and received Least Significant Bit first.
- Transmission/Receive rate is 2400 baud.
- Memory and Data bytes are sent Most Significant Byte first.

5.10.3 Entering System Monitor (Sections 3.3.1.10, 3.3.2.12)

The system monitor is entered with the following sequence:

1. Apply power to the module.
2. Transmit an "M" to the module until the module replies with a ">" prompt. The power-up reset takes approximately 1 second.
3. Transmit a "PW" as the 2 character password.
4. Once the password matches, the module will respond with a SOFTWARE VERSION LEVEL (1 byte that is 2 ASCII characters) and the result of the microcontroller's self-test ("P" = Pass, "F" = Fail). The self-test tests the internal RAM, ROM, and A/D of the microcontroller.
5. The monitor routine is now activated and ready to receive instructions.

5.10.4 System Monitor Commands

The system monitor routine will respond to three types of commands: Read, write, and jump. The following is the format for each command:

Command	Character Sent	Module Response
READ	RAAAA	DD<CR>
WRITE	WAADD	<CR>
PROGRAM	PAADD	<CR>
JUMP	JAAAA	<CR>

AA,AAA = address
DD = data
<CR> = carriage return

5 INSTRUCTIONS AND NOTES (cont'd)

5.11 Serial Communication Link (SCP)

5.11.1 General

The Serial Communication Link is a hard-wired physical interface between the tester and the DUT. The Ford SCP (Standard Corporate Protocol) Serial Communication Link, which is based on SAE J1850, uses a twisted wire pair to provide a physical communication path between a vehicle ECUs and tester connected to the Data Link. For more information about Ford SCP Serial Communications link's protocol and message structure, refer to the Subsystem Design Specification for Standard Corporate Protocol (SCP Diagnostic System (SDS-SCP-002) or latest rev.

5.11.2 Downloading Data to ECU Memory

The DUT must be placed in the Diagnostic State in order to download data into the ECU memory. The Tester must be capable of supporting and meeting all requirements related to the downloading data to ECU Memory section of the Part-One Diagnostic Specification (CPD-EESEO-VDES-001.4 or latest rev.).

In addition to the above specifications, a DUT shall meet all entry conditions specified below in order to enter into the Diagnostic State.

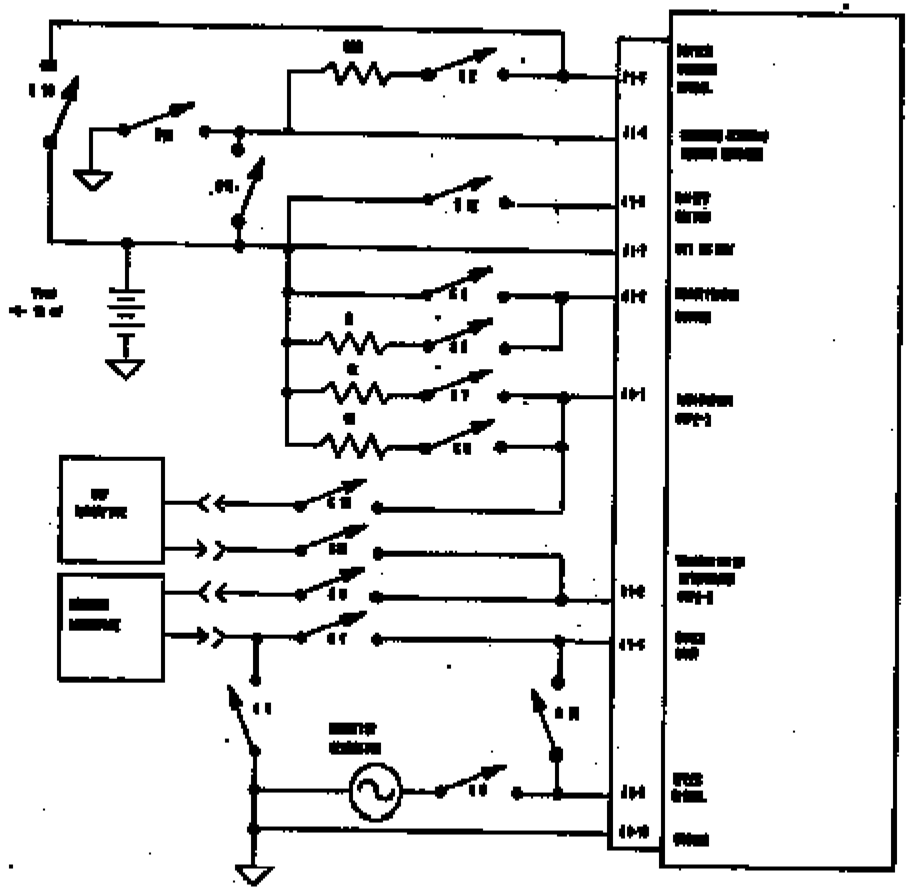
a) Power must be applied to the module.
b) DUT must receive the Park Command over the SCP Link.
c) DUT must receive a valid node-to-node message within every 5.0 seconds upon receiving the Diagnostic Command request message. Once all the data has been downloaded to the DUT's RAM, this criteria is no longer necessary since the DUT will be executing the downloaded code.

NOTE: The tester must enter into the Diagnostic State within 5 seconds of Power being applied to the module. Failure to enter into the Diagnostic State within this time will result in Fault Data being stored in the modules EEPROM.

6 COMPILATION OF REFERENCE DOCUMENTS

ES-F2VF-9A819-AA	MOUNTING ASY-SPEED CONTROL ACTU
ES-F2VF-9D864-AA	AMPLIFIER ASSEMBLY SPEED CONTROL
ES-F2AF-1316-AA	ELECTROMAGNETIC COMPATIBILITY CONFORMANCE
(SDS-SCP-002)	Subsystem Design Specification for Standard Corporate Protocol (SCP Diagnostic System)
CPD-EESEO-VDES-001.4	Part One Diagnostic Specification
Q-101 1990	FORD QUALITY CONTROL

ARRA Form #1638, or approved equivalent
FMEA Form #GPD-9368 or approved equivalent
CONTINUING PROCESS CONTROL AND PROCESS CAPABILITY IMPROVEMENT, FMC
FORD RELIABILITY METHODS, FMC



[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]

NOTE: ALL RESISTORS ARE 1%.

FUNCTIONAL TEST CIRCUIT
FIGURE 5

ENGINEERING SPECIFICATION

FIGURE 4 - FUNCTIONAL TEST STIMULUS AND MEASUREMENT MODES - FAMILY C, F, G ONLY

Test / Comments		Test No.	VPWR (+/- 0.05V)	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	OUTPUTS
				SWITCH STATES (0=OPEN / 1=CLOSED)																
Module Quiescent Current		3.3.1.1	14.00	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	I Z
Software Version		3.3.1.2	14.00	0	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	N
Micro Self Test		3.3.1.3	14.00	0	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	N
Boost. Switch Threshold	LOW	3.3.1.4.1	14.00	0	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	N
	HI	3.3.1.4.2	14.00	1	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	N
System Voltage A/D		3.3.1.5	14.00	1	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	N
Command Detect A/D	OPEN	3.3.1.6.1	14.00	1	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	N
	SET	3.3.1.6.2	14.00	1	1	1	1	0	0	0	0	1	0	0	0	0	0	0	0	N
Over Voltage		3.3.1.7	14.00	1	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	N
Oscillator		3.3.1.8	14.00	1	1	1	1	0	0	0	0	1	0	0	0	0	0	0	0	N
Set Indicator - LOGIC LEVEL ([illegible])	HI	3.3.1.9.1	14.00	1	0	1	1	0	0	1	0	1	0	0	0	0	0	0	0	V 1-10
				1	0	1	1	0	0	1	0	1	0	0	0	0	0	0	0	
Set Indicator - LAMP DRIVER ([illegible])	LOW	3.3.1.9.2	14.00	1	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	V 1-10
				1	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	
Full Load / Partial Stroke / Deactivate	RUN MODE	3.3.1.10.1	14.50	1	0	1	1	0	1	0	0	1	0	0	0	0	0	0	0	
	STROKE/PARK	3.3.1.10.2	14.50	1	0	1	1	0	1	0	0	1	0	0	0	0	0	0	0	THETA
	RELEASE	3.3.1.10.3	14.50	1	0	1	1	0	1	0	0	1	0	0	0	0	0	0	0	THETA
Full Load/Full Stroke	CLUTCH [illegible]	3.3.1.11.1	14.50	1	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	
	ENGAGE	3.3.1.11.2	14.50	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	THETA
	[illegible] PARK	3.3.1.11.3	14.50	1	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	THETA
No-Load Release/Watchdog Timeout	[illegible] LOAD	3.3.1.12.1	14.50	1	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	
	RELEASE	3.3.1.12.2	14.50	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	THETA

Generator Test Function Generator Set-Up - Families C, F, G [illegible]

Wave	Freq +/-0.01 Hz	Ampl +/- 0.01 V	Offset +/- 0.01 V	Module
Square	100.0	10 Vpp	0 V	[illegible]
Square	100.0	10 Vpp	0 V	[illegible]
Square	100.0	10 Vpp	5 V	[illegible]
Square	100.0	10 Vpp	2.5 V	[illegible]

[illegible] FOR FUNCTIONAL TEST [illegible] AND [illegible] - FAMILY [illegible] ONLY

Test / Comments		Test No.	[illegible] (+/- [illegible])	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	[illegible]
[illegible]		3.3.1.1	14.00	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	[illegible]
Software Version		3.3.1.2	14.00	0	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	[illegible]
[illegible]		3.3.1.3	14.00	0	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	[illegible]
[illegible] Switch Threshold	LOW	3.3.1.4.1	14.00	0	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	[illegible]
	HI	3.3.1.4.2	14.00	1	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	[illegible]
System Voltage A/D		3.3.1.5	14.00	1	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	[illegible]
Command Decode A/D	OPEN	3.3.1.6.1	14.00	1	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	[illegible]
	SET	3.3.1.6.2	14.00	1	1	1	1	0	0	0	0	1	0	0	0	0	0	0	0	[illegible]
Set Indicator - LAMP DRIVER (ALL FAMILY 0)	HI	3.3.1.9.1	14.00	1	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	V 1-10
	LOW	3.3.1.9.2	14.00	1	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	V 1-10
Full Load / Partial Stroke / [illegible]	[illegible]	3.3.1.10.1	14.50	1	0	1	1	0	1	0	0	1	0	0	0	0	0	0	0	
	[illegible]	3.3.1.10.2	14.50	1	0	1	1	0	1	0	0	1	0	0	0	0	0	0	0	THETA
	[illegible]	3.3.1.10.3	14.50	1	0	1	1	0	1	0	0	1	0	0	0	0	0	0	0	THETA
Full Load/Full Stroke	[illegible]	3.3.1.11.1	14.50	1	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	
	[illegible]	3.3.1.11.2	14.50	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	THETA
	[illegible]	3.3.1.11.3	14.50	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	THETA
No-Load [illegible]/[illegible] Timeout	[illegible] LOAD	3.3.1.12.1	14.50	1	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	
	[illegible]	3.3.1.12.2	14.50	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	THETA

NOTE: Function Generator not required for Diagnostic (Family [illegible]) Modules

Test / Comments	Test No.	V+BAT (+/- 0.05V)	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	OUTPUTS
FIGURE 5b - FUNCTIONAL TEST SETTINGS AND MEASUREMENT [illegible] - FAMILY H ONLY																			
Module Quiescent Current	3.3.2.1	14.00	0	0	0	0	0	0	0	0	0	1	0	0	0	0			[illegible]
Software Version	3.3.2.2	14.00	0	0	1	1	0	0	0	0	0	1	0	0	0	0			[illegible]
Micro Self Test	3.3.2.3	14.00	0	0	1	1	0	0	0	0	0	1	0	0	0	0			[illegible]
ON/OFF Switch Threshold																			
LOW	3.3.2.4.1	14.00	0	0	1	1	0	0	0	0	0	1	0	0	0	0			[illegible]
HI	3.3.2.4.2	14.00	1	0	1	1	0	0	1	0	0	1	0	1	0	0			[illegible]
2nd Command Switch Threshold																			
LOW	3.3.2.5.1	14.00	0	0	1	1	0	0	1	0	0	1	1	0	0	0			[illegible]
HI	3.3.2.5.2	14.00	0	1	1	1	0	0	0	0	0	1	0	0	0	0			[illegible]
Decel. Switch Threshold																			
LOW	3.3.2.6.1	14.00	0	0	1	1	0	0	1	1	0	1	0	0	0	0			[illegible]
HI	3.3.2.6.2	14.00	1	0	1	1	0	0	0	0	0	1	0	0	0	0			[illegible]
System Voltage A/D	3.3.2.7	14.00	1	0	1	1	0	0	0	0	0	1	0	0	0	0			[illegible]
[illegible] A/D																			
OPEN	3.3.2.8.1	14.00	1	0	1	1	0	0	0	0	0	1	0	0	0	0			[illegible]
SET	3.3.2.8.2	14.00	1	1	1	1	0	0	0	0	0	1	1	0	0	0			[illegible]
Over Voltage	3.3.1.9	16.00	1	0	1	1	0	0	0	0	1	0	0	0	0	0			[illegible]
Regulator	3.3.1.10	16.00	1	0	1	1	0	0	0	0	1	0	0	0	0	0			[illegible]
Set Indicator																			
HI	3.3.2.11.1	14.00	1	0	1	1	0	0	1	0	0	1	0	0	0	0			V 1-10
LOW	3.3.2.11.2	14.00	1	0	1	1	0	0	1	0	0	1	0	0	0	0			V 1-10
Full Load / Partial Stroke / [illegible]																			
[illegible]	3.3.2.12.1	14.50	1	0	1	1	0	1	0	0	0	1	0	0	0	0			
[illegible]	3.3.2.12.2	14.50	1	0	1	1	0	1	0	0	0	1	0	0	0	0			THETA
RELEASE	3.3.2.12.3	14.50	1	0	1	1	0	1	0	0	0	1	0	0	0	0			THETA
Full Load / Full Stroke																			
CLUTCH [illegible]	3.3.2.13.1	14.50	1	0	1	1	0	0	0	0	0	1	0	0	0	0			
[illegible]	3.3.2.13.2	14.50	1	0	0	0	0	0	0	0	0	1	0	0	0	0			THETA
[illegible]	3.3.2.13.3	14.50	1	0	0	0	1	0	0	0	0	1	0	0	0	0			THETA
No-Load Release/[illegible] Thrust																			
[illegible]	3.3.2.14.1	14.50	1	0	0	0	1	0	0	0	0	1	0	0	0	0			
RELEASE	3.3.2.14.2	14.50	1	0	0	0	0	0	0	0	0	1	0	0	0	0			THETA

Regulator Test Function Generator Set-Up - Family H				
Wave	Freq +/- 0.01 Hz	Ampl +/- 0.01 V	Offset +/- 0.01 V	Module
Square	100.0	10 Vpp	2.4 V	All

ENGINEERING SPECIFICATION

PART NUMBER [illegible]-9C735-AA

REV

3718 7202

FIGURE 4c - FUNCTIONAL TEST STIMULUS AND [illegible] - FAMILY [illegible] ONLY

Test / Comments		Test No.	VOLTS (+/- 0.0V)	SWITCH STATES (0=OPEN / 1=CLOSED) S1 S2 S3 S4 S5 S6 S7 S8 S9 S10 S11 S12 S13 S14 S15 S16	OUTPUTS
Module Quiescent Current		3.3.3.1	14.00	1 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0	[illegible]
Software Version		3.3.3.2	14.00	0 0 0 0 0 0 0 0 0 1 0 0 0 0 1 1	[illegible]
Micro Self Test		3.3.3.3	14.00	0 0 0 0 0 0 0 0 0 1 0 0 0 0 1 1	[illegible]
Boost Switch Threshold	LOW	3.3.3.4.1	14.00	0 0 0 0 0 0 0 0 0 1 0 0 0 0 1 1	[illegible]
	HI	3.3.3.4.2	14.00	1 0 0 0 0 0 0 0 0 1 0 0 0 0 1 1	[illegible]
System Voltage A/D		3.3.3.5	14.00	1 0 0 0 0 0 0 0 0 1 0 0 0 0 1 1	[illegible]
Command Decode A/D	OPEN	3.3.3.6.1	14.00	1 0 0 0 0 0 0 0 0 1 0 0 0 0 1 1	[illegible]
	SET	3.3.3.6.2	14.00	1 1 0 0 0 0 0 0 0 1 0 0 0 0 1 1	[illegible]
Full Load / Partial Stroke / Reactivate	[illegible] BOOT	3.3.3.7.1	14.50	1 0 0 0 0 1 0 0 0 1 0 0 0 0 1 1 1 0	
	[illegible]	3.3.3.7.2	14.50	0 0 0 1 0 0 0 1 0 0 0 0 1 1	THETA
	RELEASE	3.3.3.7.3	14.50	1 0 0 0 0 1 0 0 0 1 0 0 0 0 1 1	THETA
Full Stroke / Full Load	CLUTCH DWELL	3.3.3.8.1	14.50	1 0 0 0 0 0 0 0 0 1 0 0 0 0 1 1	
	STROKE	3.3.3.8.2	14.50	1 0 0 0 0 0 0 0 0 1 0 0 0 0 1 1	THETA
	SERVO MAX	3.3.3.8.3	14.50	1 0 0 0 1 0 0 0 0 1 0 0 0 0 1 1	THETA
No-Load Release/Watchdog Timeout	REMOVE LOAD	3.3.3.9.1	14.50	1 0 0 0 1 0 0 0 0 1 0 0 0 0 1 1	
	RELEASE	3.3.3.9.2	14.50	1 0 0 0 0 0 0 0 0 1 0 0 0 0 1 1	THETA

[illegible] Test Function Generator Set-Up - Family [illegible]

Wave	Freq +/- 0.01 Hz	Ampl +/- 0.01 V	Offset +/- 0.01 V	Module
Square	100.0	10 Vpp	0 V	All
Square	100.0	10 Vpp	5 V	

FIGURE 4 - FUNCTIONAL TEST STIMULUS AND MEASUREMENT POINTS - FAMILY C, F, G ONLY

Test / Comments		Test No.	VPWR (+/- 0.05V)	Switch [illegible] / 1=CLOSED																Output
				[illegible]																
Module Quiescent Current		3.3.1.1	14.00	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	I 7
Software Version		3.3.1.2	14.00	0	0	1	1	0	1	0	0	1	0	0	0	0	0	0	0	[illegible]
Micro Self Test		3.3.1.3	14.00	0	0	1	1	0	1	0	0	1	0	0	0	0	0	0	0	[illegible]
Temp. Switch Threshold	LOW	3.3.1.4.1	14.00	0	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	[illegible]
	HI	3.3.1.4.2	14.00	1	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	[illegible]
System Voltage A/D		3.3.1.5	16.00	1	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	[illegible]
Command Decode A/D	[illegible]	3.3.1.6.1	14.00	1	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	[illegible]
	SET	3.3.1.6.2	16.00	1	1	1	1	0	0	0	0	1	0	0	0	0	0	0	0	[illegible]
Over Voltage		3.3.1.7	14.00	1	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	[illegible]
Resonator		3.3.1.8	14.00	1	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	[illegible]
Set Indicator - LOGIC LEVEL ([illegible])	HI	3.3.1.9.1	14.00	1	0	1	1	0	0	1	0	1	0	0	0	0	0	0	0	V 1-10
	LOW	3.3.1.9.2	14.00	1	0	1	1	0	0	1	0	1	0	0	0	0	0	0	0	V 1-10
Set Indicator - LAMP DRIVER ([illegible])				1	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	
				1	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	
Full Load / Partial Stroke / Reactivate	[illegible]	3.3.1.10.1	14.50	1	0	1	1	0	1	0	0	1	0	0	0	0	0	0	0	
	[illegible]	3.3.1.10.2	14.50	1	0	1	1	0	1	0	0	1	0	0	0	0	0	0	0	[illegible]
	RELEASE	3.3.1.10.3	14.50	1	0	1	1	0	1	0	0	1	0	0	0	0	0	0	0	[illegible]
Full Load/Full Stroke	[illegible]	3.3.1.11.1	14.50	1	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	
	STROKE	3.3.1.11.2	14.50	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	[illegible]
	[illegible]	3.3.1.11.3	14.50	1	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	[illegible]
No-Load Release/Watchdog Timeout	[illegible]	3.3.1.12.1	14.50	1	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	
	RELEASE	3.3.1.12.2	14.50	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	[illegible]

Resonator Test Function Generator Set-Up - Families C, F, G [illegible]

Wave	Freq +/-0.01 Hz	Ampl +/- 0.01 V	Offset +/- 0.01 V	Module
Square	100.0	10 Vpp	0 V	[illegible]
Square	100.0	10 Vpp	0 V	[illegible]
Square	100.0	10 Vpp	5 V	[illegible]
Square	100.0	10 Vpp	2.5 V	[illegible]

ENGINEERING SPECIFICATION

PART NUMBER [illegible]

REV

FIGURE 5x - Functional Test Limits (-40C to 85C) - Family [illegible] (Diagnostics) Only

Modules: [illegible]

Test	No.	Outputs	Min	Target @ 25° C	Max	Comments	Unit
Quiescent Current	3.3.1.1	I 1-7	17	25	32		mA
Software Version	3.3.1.2	N	-	As Req'd	-	* See Figure 19x	*
[illegible] Self Test	3.3.1.3	N	-	0	-		P/F
Deactivator Switch Threshold [illegible] [illegible]	 3.3.1.4.1 3.3.1.4.2	 N N	 - -	 0 1	 - -		 P/F P/F
System Voltage A/D	3.3.1.5	N	176	180	187		counts
Command Decode OPEN CIRCUIT "[illegible]" [illegible]	 3.3.1.6.1 3.3.1.6.2	 N N	 -5 -77	 0 -72	 5 -67		 counts counts
Set Indicator [illegible] [illegible]	 3.3.1.9.1 3.3.1.9.2	 V 1-10 V 1-10	 [illegible] 0	 13.71 0.35	 14.65 0.40		 V V
Full Load / Partial Stroke / Reactivate [illegible] [illegible] [illegible]	 3.3.1.10.1 3.3.1.10.2 3.3.1.10.3	 THETA THETA	 31 -5	 31 0	 36 5		 Deg. Deg.
Full Load / Full Stroke [illegible] [illegible] [illegible]	 3.3.1.11.1 3.3.1.11.2 3.3.1.11.3	 THETA	 169	 179	 183		 Deg.
No Load Release and Unlatching Timeout [illegible] RELEASE	 3.3.1.12.1 3.3.1.12.2	 THETA	 -5	 0	 5		 Deg.

FIGURE 3b - FUNCTIONAL TEST LIMITS (-40C to 125C) - [illegible]

Test		No.	Outputs	Min	Target @ 25° C	Max	Comments	Unit
Quiescent Current		3.3.2.1	I 1-7	17	22	32		mA
Software Version		3.3.2.2	N	-	As Req'd	-	* See Figure 11b	*
Micro Self Test		3.3.2.3	N	-	P	-		P/F
ON/OFF Switch Threshold	LOW	3.3.2.4.1	N	-	0	-		P/F
	HI	3.3.2.4.2	N	-	1	-		P/F
2nd Com. Switch Threshold	HI	3.3.2.5.1	N	-	1	-		P/F
	LOW	3.3.2.5.2	N	-	0	-		P/F
Dec. Switch Threshold	LOW	3.3.2.6.1	N	-	0	-		P/F
	HI	3.3.2.6.2	N	-	1	-		P/F
System Voltage A/D		3.3.2.7	N	174	185	197		counts
Command Decode	OPEN CIRCUIT	3.3.2.8.1	N	-5	0	5		counts
	"OFF" COMMAND	3.3.2.8.2	N	-77	-72	-67		counts
Over Voltage		3.3.2.9	N	45	50	55		counts
Resonator		3.3.2.10	N	3.992	4.000	4.008		MHz
Set Indicator	ON	3.3.2.11.1	V 1-16	13.40	13.71	14.05		V
	LOW	3.3.2.11.2	V 1-16	0	0.35	0.60		V
Full Load / Partial Stroke / Dwell Time	[illegible]	3.3.2.12.1						
	[illegible]	3.3.2.12.2	Tests	21	31	34		Deg.
	[illegible]	3.3.2.12.3	Tests	-5	0	5		Deg.
Full Load / Full Stroke	CLUTCH [illegible]	3.3.2.13.1						
	STROKE	3.3.2.13.2						
	SERVO PARK	3.3.2.13.3	Tests	160	170	180		Deg.
No Load Release and Latching Timeout	[illegible]	3.3.1.14.1						
	RELEASE	3.3.1.14.2	Tests	-5	0	5		Deg.

ENGINEERING SPECIFICATION

PART NUMBER ES-F2??-9C735-AA

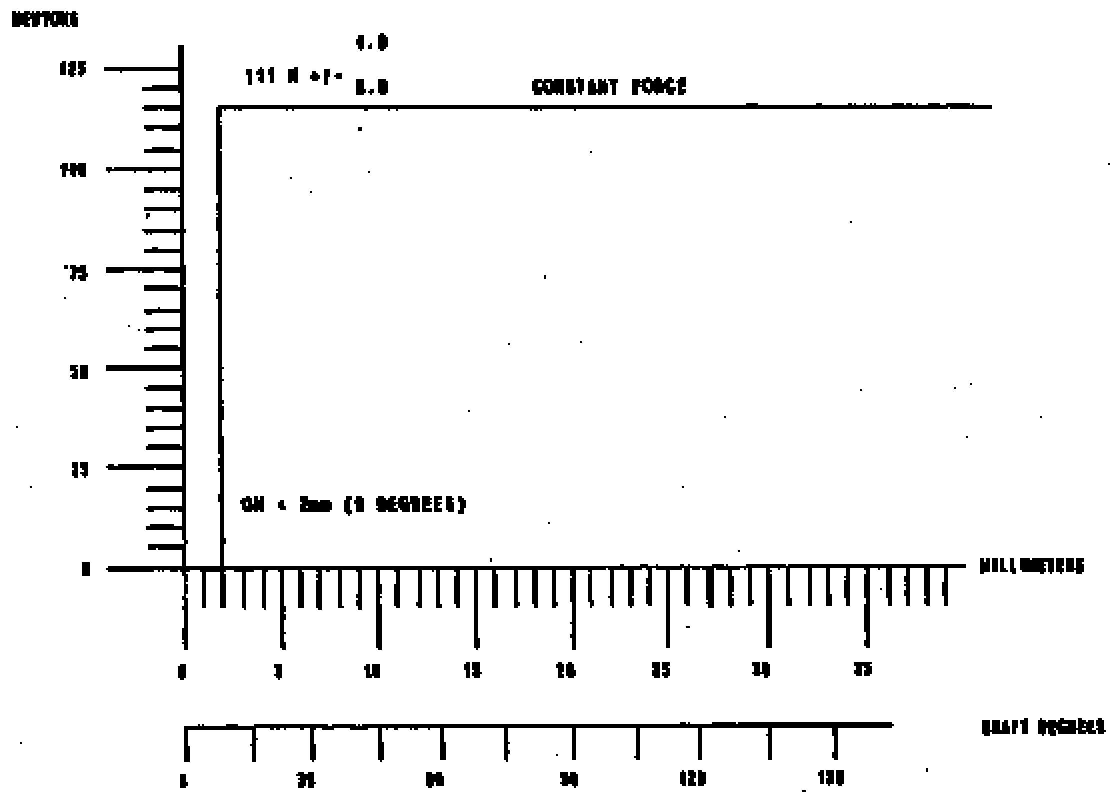
REV

PAGE 43

FIGURE [illegible] - Functional Test Limits (-40C to 125C) - Family [illegible] Only

Module: [illegible]

Test	No.	Outputs	Min	Target @ 25° C	Max	Comments	Unit
Solenoid Current	3.3.3.1	I 1-7	17	24	32		mA
Software Version	3.3.3.2	N	-	As Req'd	-	* See Figure [illegible]	*
Micro Self Test	3.3.3.3	N	-	P	-		P/F
Deactivator Switch Threshold LOW HI	 3.3.3.4.1 3.3.3.4.2	 N N	 - -	 0 1	 - -		 P/F P/F
System Voltage A/D	3.3.3.5	N	174	185	197		counts
Command Decode OPEN CIRCUIT "SET" COMMAND	 3.3.3.6.1 3.3.3.6.2	 N N	 -5 -77	 0 -72	 5 -67		 counts counts
Full Load / Partial Stroke / Deactivate RAM TEST STROKE/PARK RELEASE	 3.3.3.7.1 3.3.3.7.2 3.3.3.7.3	 THETA THETA	 21 -5	 31 0	 34 3		 Deg. Deg.
Full Load / Full Stroke CLUTCH DWELL STROKE SERVO PARK	 3.3.3.8.1 3.3.3.8.2 3.3.3.8.3	 THETA	 160	 170	 180		 Deg.
No Load Release and Unwinding Timeout STROKE LOAD RELEASE	 3.3.3.9.1 3.3.3.9.2	 THETA	 -5	 0	 5		 Deg.



LOAD LINE

FIGURE 6

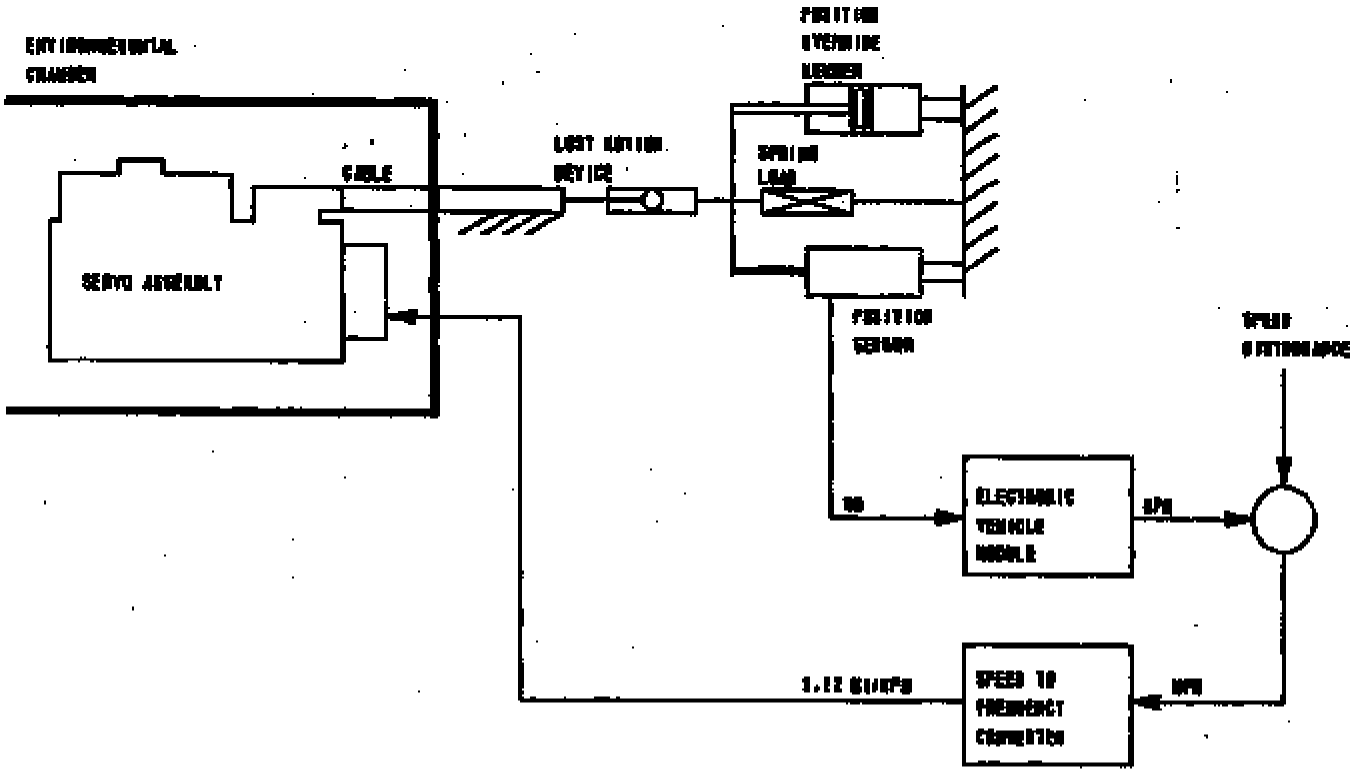
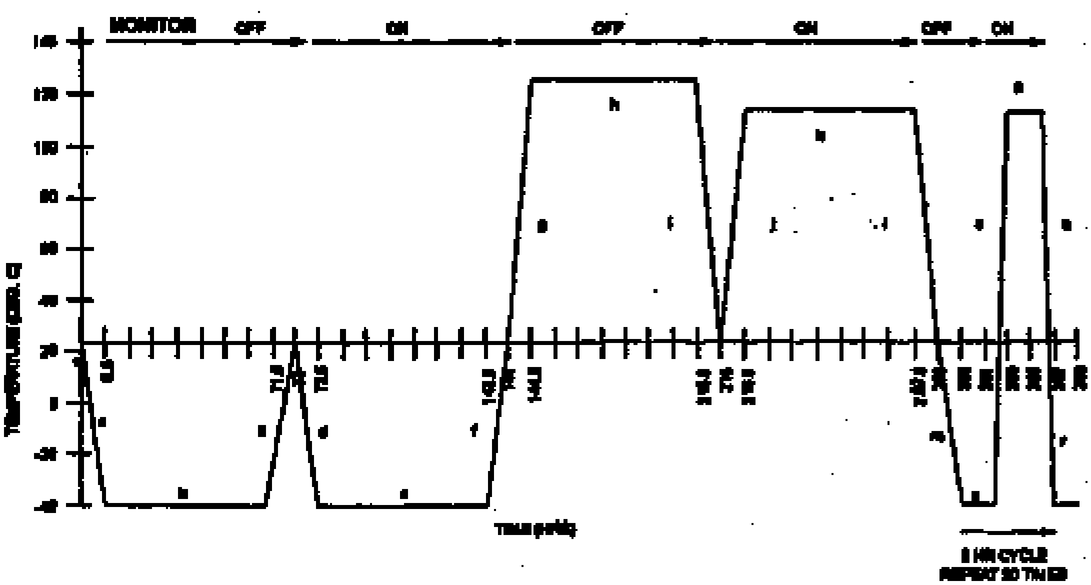


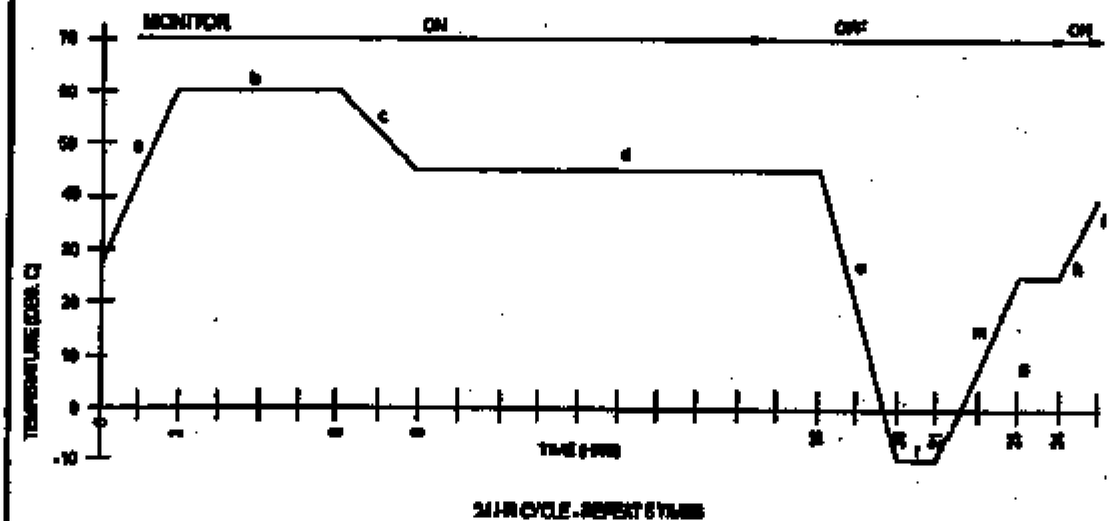
FIGURE 7



MONITORED CLIMATIC ENVIRONMENT TESTS
FIGURE 8

SEGMENT	ACTION	DWELL	CUMULATIVE TIME	MONITOR	SYSTEM VOLTAGE
a	Cool from 25°C to -40°C	0.5	0.5	off	13.25
b	Hold at -40°C	71	71.5	off	15.5
c	Heat from -40°C to 25°C	0.5	72	off	15.25
d	Cool from 25°C to -40°C	0.5	72.5	on	15.25
e	Hold at -40°C	71	143.5	on	15.5
f	Heat from -40°C to 25°C	0.5	144	on	13.25
g	Heat from 25°C to 125°C	0.5	144.5	off	13.5
h	Hold at 125°C	71	215.5	off	12.5
i	Cool from 125°C to 115°C	0.5	216	off	13.5
j	Heat from 25°C to 115°C	0.5	216.5	on	13.5
k	Hold at 115°C	71	287.5	on	12.5
l	Cool from 115°C to 25°C	0.5	288	on	13.5
m	Cool from 25°C to -40°C	1	289	off	13.25
n	Hold at -40°C	2	291	off	15
o	Heat from -40°C to 115°C	2	293	on	13.5
p	Hold at 115°C	2	295	on	12.5
q	Cool from 115°C to 25°C	1	296	on	13.5
r	(repeat m thru q 30 times)	232	528	-	-

FIGURE 8a
MONITORED CLIMATIC ENVIRONMENT TEST CYCLE



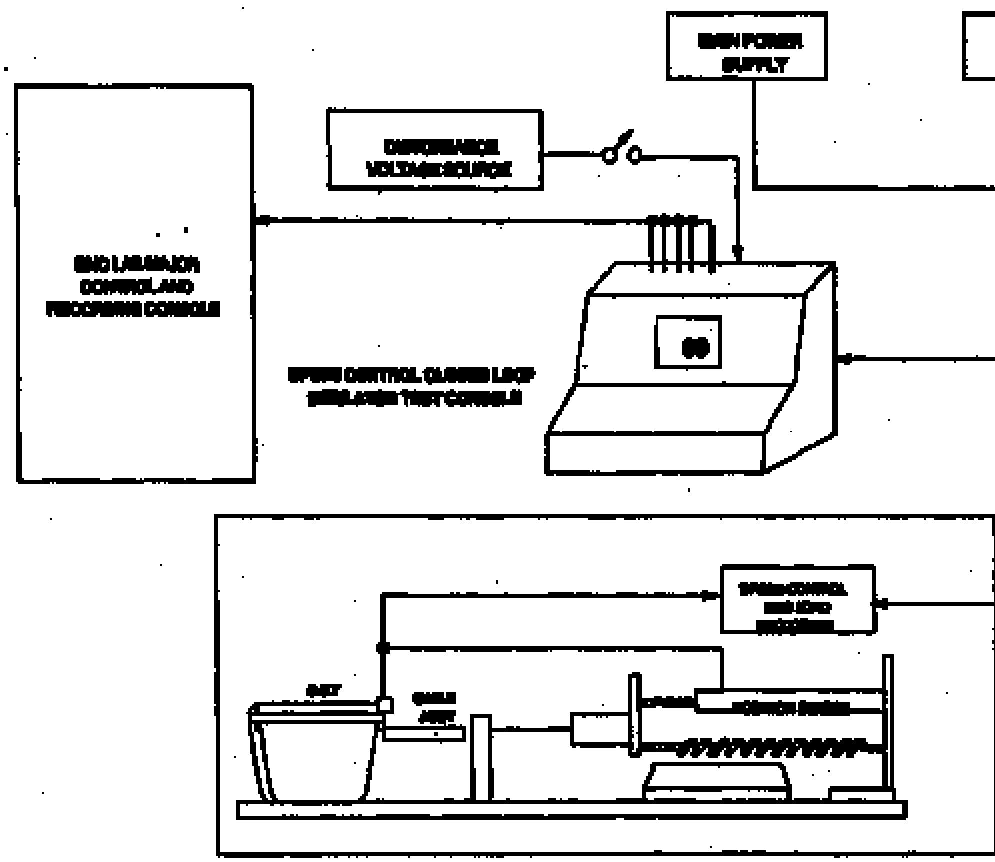
HUMIDITY-TEMPERATURE ENVIRONMENT TEST CYCLE
FIGURE 9

SEGMENT	ACTION	RELATIVE HUMIDITY	DWELL	CUMULATIVE TIME	MONITOR
a	Heat from 25°C to 60°C		2	2	on
b	Hold at 60°C	90%	4	6	on
c	Cool from 60°C to 45°C		2	8	on
d	Hold at 45°C	95%	10	18	on
e	Cool from 45°C to -10°C		2	20	off
f	Hold at -10°C		1	21	off
g	Heat from -10°C to 25°C		2	23	off
h	Hold at 25°C		1	24	off
i	(repeat a thru h 5 times)		120	-	-

FIGURE 9a

HUMIDITY-TEMPERATURE ENVIRONMENT TEST CYCLE

3718 7211



EMC SCREEN ROOM TEST CELL
FIGURE [illegible]

FIGURE 11

SPEED CONTROL INITIALIZATION/SET-UP FOR EMC TESTS

INITIALIZATION

(Applicability: RI01-1, RI02, RI03, CI01-1A, CI01-1B, CI02-1A, CI02-1B, CI02-2, CI02-3A, CI02-3B, CI02-4, CI04, RE01, CE01)

1. Note the amplifier model type and set up the appropriate external speed signal type from the frequency generator per Figure 4, 4a, 4b, or 4c. Set at 100 Hz.

2. With the main power supply disconnected from the battery, set the power supply voltage to 12.7 +/- 0.1 Volts and the current limit set to 4 amps. Reconnect the power supply to the Speed Control Simulator Console and storage battery.

3. Turn on power to the module under test and Speed Control Console via console panel switch.

4. Momentarily depress the "SET" button and wait until the pointer on the Speed Control fixture advances, then stabilizes.

5. Adjust the pointer gage such that the pointer is in the center of the gage.

6. Adjust the video monitor so that the pointer/gage can be observed.

7. With the Speed Control set at 100 Hz, verify the main power has settled and at a steady 12.7 +/- 0.1 Volts. This settling may take a few minutes as the battery voltage stabilizes to match the power supply setting.

8. Proceed with test according to EMC specification ES-F2AF-1316-AA.

DURING TEST

(Applicability: RI01-1, RI02, RI03, CI01-1A, CI01-1B, CI02-1A, CI02-1B, CI02-2, CI02-3A, CI02-3B)

1. Apply "BRAKE" command from Speed Control Console and verify pointer returns to idle stop position through video monitor.

SET-UP: CI02-5 (LOAD DUMP) CI02-6 (GROUND SHIFT) and CI03-1 (REVERSE BATTERY)

1. Apply Power to Pins 7, 9, Ground to Pin 10. For Family "H", also apply Power to Pin 8.

SET-UP: CI04-1 (ESD-UNPOWERED)

1. Discharge to 10 Pin connector only.

SET-UP: CI04-2 (ESD-OPERATING)

1. Discharge to Pins 5 and 6 only. For Family "H" also discharge to Pin 8.

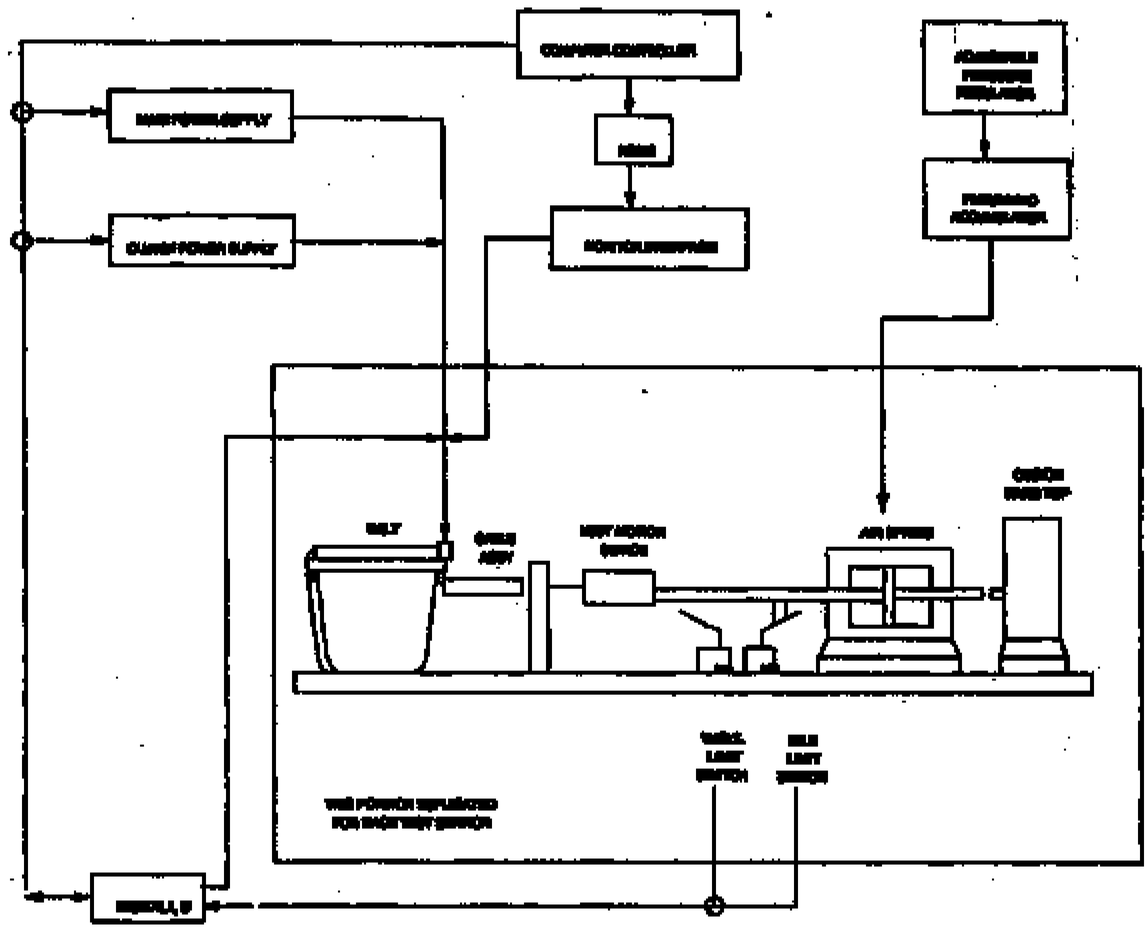


FIGURE 18

FIGURE 13

Accelerated Life Test Parameters

EQUIPMENT DESCRIPTION:

Computer Controller: Minimum - Capable of controlling two power supplies, scanning and driving digital I/O, driving an RS232 line and transmitting an ASCII file to boot the Device Under Test (D.U.T.).

Main Power Supply: Minimum - Preferably computer controllable, Voltage range adjustable 0 to 30V and output current capacity of 3A per test station.

Clutch Power Supply: Minimum - Preferably computer controllable, Voltage range adjustable 0 to 30V and output current capacity of 3A per test station.

Digital I/O: Minimum per station - Capable of driving the D.U.T. brake input and disconnecting from the brake input. Also capable of scanning two limit switches per station.

Monitor Interface: Minimum - Capable of converting the ASCII transmission from the computer to the voltage levels needed by the D.U.T.. It must be capable of disconnecting from the D.U.T..

Limit Switches: Two per station - One to determine the idle position of the D.U.T. within 3mm. The other can determine the full stroke position within 3mm.

Pressure Regulator: Sets the pull force of the air spring by allowing air to flow into the system if the pressure falls below the set pressure. Note, this is a one way process. Should the pressure in the system increase, it does not allow air to back flow into the air supply. Some regulators will vent air to the atmosphere but this is a poorly regulated function and is more of a safety relief then regulation.

Air Spring: An air cylinder having low static friction and pressurized to resist the pulling action of the D.U.T.. Using the air pressure regulator, it should have an adjustable pull force ranging from 10 to 40 pounds and a minimum usable stroke range of 3 inches.

FIGURE 11 (cont'd)

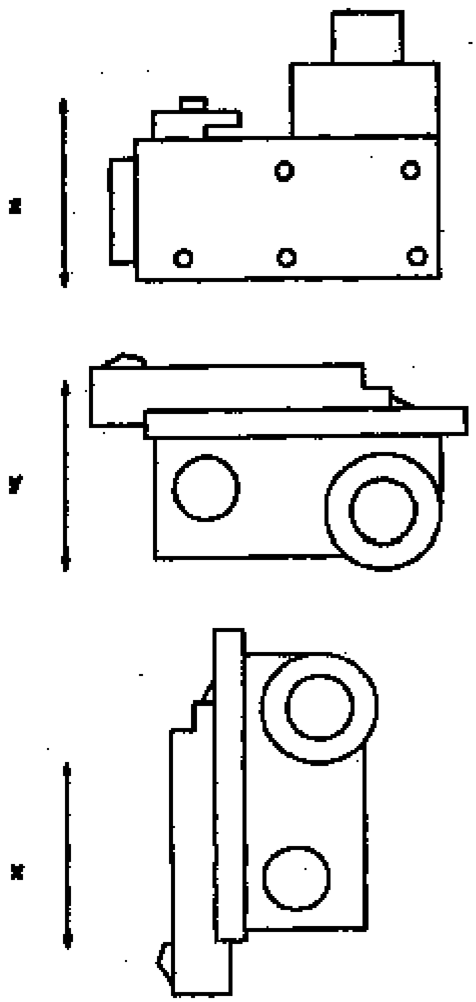
1000 Hour Accelerated Life Test Parameters

EQUIPMENT DESCRIPTION (cont'd):

Accumulator: The accumulator lowers the rate of the air spring allowing it to have a near constant force over its full stroke. For example: If an air spring displaces 2 cubic inches of air and the accumulator contains 98 cubic inches of air, then the force of the spring will vary 2/(98+2) or 2% over the 2 inch stroke.

Also, the reservoir is used to supply the large demand for air when the D.U.T. allows the spring to snap against the hard stop/cushion. For example: If the air spring snaps into the hard stop in 10 mS and its displacement is 2 cubic inches, then the demand for air will be 2/.01 = 200 cubic inches/second. Because of this large flow rate the line between the air spring and the accumulator should be as large a size as practical and length should be kept to a minimum. If the areas of both sides of the air cylinder are equal, then the air on the back side of the piston must be allowed to escape at the same 200 cubic inches per second rate.

Cushion/Hard Stop: A device which prevents the air spring from transmitting static or dynamic force to the actuator when the D.U.T. is in its free deactivated position. The cushion action prevents damage to the fixture when the D.U.T. allows the air spring to snap into the hard stop position. The cushion action should occur only within 100 mils or less of the hard stop position of the fixture.



AXIS OF VIBRATION
FIGURE 14

FIGURE 15

SERVO FUNCTIONAL TEST DOWNLOAD CODE

BASE MODULE - B4 MICROPROCESSOR (MONITOR FILE B4MTR19.MON)						
W8D3F	W9700	WA173	WAB0C	WB550	WBF3A	WC9CC
W8E3F	W98B7	WA2A6	WAC03	WB6A6	WC051	WCA20
W8F30	W9973	WA334	WAD00	WB7FF	WC126	WCB02
W9017	W9AA6	WA420	WAE0D	WB8B7	WC202	WCC20
W9156	W9B3A	WA500	WAF0F	WB951	WC31E	WCDFE
W9216	W9C20	WA6B7	WB050	WBA20	WC450	J008D
W9375	W9D08	WA774	WB102	WBB09	WC50C	
W9418	W9EA6	WA81D	WB250	WBC0E	WC600	
W9575	W9FD2	WA975	WB35C	WBD50	WC7C8	
W96A6	WA0B7	WAA19	WB43F	WBE06	WC820	

BASE MODULE - F6 MICROPROCESSOR (MONITOR FILE F6MTR19.MON)						
W8D5F	W9700	WA174	WABC7	WB55C	WBF50	WC9GA
W8E3F	W98B7	WA2A6	WAC1F	WB63F	WC006	WCA20
W8F50	W9974	WA334	WADF0	WB750	WC13A	WCBCA
W9017	W9AA5	WA420	WAE0A	WB8A6	WC251	WCC20
W9157	W9B54	WA500	WAF00	WB9FF	WC326	WCD00
W9216	W9C20	WA6B7	WB000	WBAB7	WC402	WCE20
W9376	W9D08	WA775	WB10F	WBB51	WC51E	WCFFE
W9418	W9EA5	WA81D	WB250	WBC20	WC650	J004D
W9576	W9F02	WA976	WB302	WBD09	WC7DC	
W96A6	WA0B7	WAA4F	WB43C	WBE0E	WC800	

DIAGNOSTIC MODULE - F6 MICROPROCESSOR						
W8E5F	W9800	WA276	WACC7	WB65C	WC050	WCAC8
W8F3F	W99B7	WA3A6	WAD1F	WB73F	WC106	WCB20
W9050	W9A76	WA434	WAEF0	WB850	WC23A	WCCCA
W9117	W9BA6	WA520	WAF0A	WB9A6	WC351	WCD20
W9250	W9C34	WA600	WB000	WBAFF	WC426	WCED0
W9316	W9D20	WA7B7	WB10D	WBBB7	WC502	WCF20
W9478	W9E06	WA877	WB20F	WBC51	WC61E	WD0FE
W9518	W9FA6	WA91D	WB350	WBD20	WC750	J004E
W9678	WA002	WAA78	WB402	WBE09	WC8DC	
W97A6	WA1B7	WAB4F	WB55C	WBF0E	WC900	

FIGURE 16

SERVO MONITORED INSTABILITY TEST DOWNLOAD CODE

FAMILY C,F,G (BASE) MODULE - P6 MICROPROCESSOR						

FAMILY D (DIAGNOSTIC) MODULE - P6 MICROPROCESSOR						

FAMILY M (MAZDA) MODULE - P6 MICROPROCESSOR						

FAMILY U (SCP) MODULE - P6 MICROPROCESSOR						

FIGURE 17

SERVO ACCELERATED LIFE TEST DOWNLOAD CODE

BASE MODULE - 34 MICROPROCESSOR (MONITOR FILE ADT5.MON)

W8D17	W993F	WA57A	WB126	WBD87	WC9A6	WD5B1	WE120
W8E56	W9A74	WA617	WB2FB	WBE74	WCA00	WD683	WE2AC
W8FAD	W9BAD	WA775	WB316	WBFAD	WCB87	WD726	WE310
W9052	W9C46	WA818	WB475	WC022	WCC73	WD8F0	WE40C
W9182	W9D03	WA975	WB5AD	WC102	WCDA6	WD9B6	WE50D
W9200	W9E08	WAA16	WB620	WC200	WCE60	WDA74	WE675
W93FB	W9FF9	WAB00	WB7A6	WC3FB	WCF87	WDB81	WE7FB
W94AD	WA0AD	WACAE	WB801	WC4AD	WD074	WDC84	WE81D
W954D	WA141	WAD02	WB987	WC51D	WD1AD	WDD26	WE975
W9602	WA23D	WAEAD	WBA73	WC602	WD210	WDEEA	WEA81
W9700	WA384	WAF33	WBBA6	WC700	WD386	WDF17	J008D
W98F6	WA426	WB05A	WBCE0	WC8F6	WD473	WE000	

BASE MODULE - F6 MICROPROCESSOR (MONITOR FILE F6ADT5.MON)

W8D17	W993F	WA5FA	WB126	WBD87	WC9A6	WD5B1	WE120
W8E57	W9A75	WA617	WB2FB	WBE75	WCA01	WD686	WE2AC
W8FAD	W9BAD	WA776	WB316	WBFAD	WCB87	WD726	WE34F
W9052	W9C46	WA81B	WB476	WC022	WCC74	WD8F0	WE4C7
W910B	W9D0A	WA976	WB5AD	WC10B	WCDA6	WD9B6	WE51F
W9200	W9E00	WAA18	WB62C	WC200	WCE50	WDA75	WE6F0
W93FB	W9FF9	WAB00	WB7A6	WC3FB	WCF87	WDB81	WE700
W94AD	WA0AD	WACAE	WB801	WC4AD	WD075	WDC87	WE876
W954D	WA141	WAD02	WB987	WC51D	WD1AD	WDD26	WE9F9
W9608	WA23D	WAEAD	WBA74	WC60B	WD210	WDEEA	WEA1D
W9700	WA387	WAF33	WBBA6	WC700	WD386	WDF17	WEB76
W98F6	WA426	WB05A	WBCE0	WC8F6	WD474	WE000	WEC81
							J008D

DIAGNOSTIC MODULE - F6 MICROPROCESSOR

W8E17	W9A3F	WA6FA	WB2AD	WBE0B	WCAA6	WD6B6	WE2C7
W8F59	W9B77	WA717	WB32D	WBF00	WCB50	WD777	WE31F
W90AD	W9CAD	WA878	WB4A6	WC0FB	WCCB7	WD8B1	WE4F0
W914F	W9D43	WA918	WB501	WC1AD	WCD77	WD989	WE50D
W920B	W9E0A	WAA78	WB6B7	WC21E	WCEAD	WDA26	WE678
W9300	W9F00	WABC0	WB776	WC30B	WCF11	WDBEA	WE7F9
W94FB	WA0F9	WAC01	WB8A6	WC400	WD0B6	WDCCD	WE81D
W95AD	WA1AD	WAD11	WB9E0	WC5F6	WD176	WDD01	WE976
W964A	WA23E	WAEAD	WBAB7	WC6A5	WD2B1	WDE14	WEA81
W970B	WA33D	WAF91	WBB77	WC701	WD388	WDF20	J008D
W98D0	WA489	WB016	WBCAD	WC8B7	WD428	WE0AF	
W99F6	WA526	WB178	WBD23	WC976	WD5F0	WE14F	

FIGURE 18

MONITORED DURABILITY I/O DEFINITION

I/O DEFINITION		
INPUT/OUTPUT	**VALUE**	
B - Brake	L = Logic Low Ind. Lamp = OFF	H = Logic High Ind. Lamp = ON
A = Speed C = On/Off Switch (FAMILY "M" ONLY) D = De-Activator Switch J = Clutch Switch (FAMILY "M" ONLY)	L = Logic Low L = Logic Low L = Logic Low L = Logic Low	H = Logic High H = Logic High H = Logic High H = Logic High
G = Command Switch	A/D Conversion of Command Input: 00h to 48h = "CANCEL" 49h to A7h = "SET/COAST" (240 ohm) A8h to DAh = "RESUME/ACCEL" DBh to F7h = "NULL" Command (open ckt) F8h to FFh = "FAULT"	

ENGINEERING SPECIFICATION	PART NUMBER [illegible]	REV	FRAME 59

FIGURE [illegible] Test [illegible] Software Version Families [illegible]				FIGURE [illegible] Test [illegible] Software Version Family [illegible]		FIGURE [illegible] Test [illegible] Software Version Family [illegible]		FIGURE [illegible] Test [illegible] Software Version Family [illegible]	
[illegible] Type	Version	[illegible] Type	Version	[illegible] Type	Version	[illegible] Type	Version	[illegible] Type	Version
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]		
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[illegible]	[illegible]								
[illegible]	[illegible]								

ENGINEERING SPECIFICATION

PART NAME	PART NUMBER
SPECIFICATION - SPEED CONTROL ASSEMBLY	ES-F2VF-9A819-AA

LET	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
FR	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
LET	C	C	C	C	C	C	C	C	C	C	C	C	C	C			
FR	18	19	20	21	22	23	24	25	26	27	28	29	30	31			
LET																	
FR																	
LET																	
FR																	
LET																	
FR																	
LET																	
FR																	

DATE	LET	FR	REVISIONS	DR	CK
			C. WEBER (313) 845-1495		
910404			PROD REL DR00-E-10023510-000		
	A	ALL	REVISED AND RENUMBERED FRAMES		
	A		C. WEBER (313) 845-1495		
911111	A		C-10154393		
	B	9-31	REVISED TO AGREE WITH S.R.E.A.'S & RENUMBERED FRAMES 9-31		
	B		D. PORTER (313) 390-8674		
940513	B		PROD REL DR00-E-00107002-197		
	C	ALL	REDRAWN, REVISED AND RENUMBERED		
	C		D. PORTER (313) 390-8674		
[illegible]	C		REL DR00-E-10020356-000		[illegible]

REFERENCE	
PREPARED/APPROVED BY	
CHECKED BY	DETAILED BY (ON FILE)
CONCURRENCE/APPROVED SIGNATURES	
DESIGN ENGINEER SUPV. (ON FILE)	
DESIGN ENGRG. MGMT. (ON FILE)	
MANUFACTURING ENGRG.	
QUALITY CONTROL (ON FILE)	
PURCHASING	
SUPPLIER QUALITY ASSISTANCE	

FRAME 1 OF 31 | REV C

TABLE OF CONTENTS

TABLE OF CONTENTS (cont'd)

1 GENERAL

This specification governs the speed control assembly. The actuator subassembly is comprised of a housing with integrated motor, a clutch assembly gears and cable pulley.

This Engineering Specification is a supplement to the released drawing on the released part, and all requirements herein must be met in addition to all other requirements of the part drawing. Minimum measures necessary for demonstrating compliance to these requirements are given in each section.

The Engineering Specification is intended to evaluate specific characteristics as a supplement to normal material inspections dimensional checking, and in-process controls, and should in no way adversely influence other inspection operations.

Preparation and submission of an acceptable Control Plan are the responsibility of the manufacturing source. Control Plan approval by the Component Engineering and Manufacturing Operations and by other activities according to QS-9000 is a prerequisite for initial sample review and approval. The manufacturing source will retain the original of the approved Control Plan and any later revisions per QS-9000 and provide a copy to the design responsible CEMO.

2 SUMMARY OF PRODUCTION VALIDATION AND IN PROCESS TESTS

Production Validation (PV) tests are used to obtain an initial estimate of the process potential to produce parts that conform the engineering requirements, and to identify causal or predictive relationships between significant design and process characteristics (to be used for process control). These tests must be completed satisfactorily using initial parts from production tooling and processes before Initial Sample Report (PSW) approval and authorization of production parts can be issued. Sampling plans for PV testing must be included in the Control Plan.

In-Process (IP) tests are used to further understand the relationship between significant design and process characteristics and to establish a basis for continuing improvement. Tests must be completed with production parts on an ongoing basis. Sampling plans for both IP testing and evaluation of the significant process characteristics must be included in the Control Plan. When the process is found to be out of control or the test acceptance criteria are not met, the reaction plan approved in the Control Plan shall be invoked.

PRODUCTION VALIDATION AND IN-PROCESS TESTS
FIGURE 1

TEST NUMBER	TEST CHARACTERISTIC	TEST USE	TEST LIMITS (OVER SPECIFIED TEMPERATURE) MIN	TARGET	MAX		MINIMUM CONFORMANCE TO TOLERANCE	SUGGESTED* SAMPLE SIZE /FREQUENCY
	Lot Control:							
III.B	Functional Tests							
III.B.1	Clutch Assembly Functional	PV/IP						6/shift/line
III.B.1.a	Dielectric Test		-	-	95	mA	2/	
III.B.1.b.1	Coil Resistance at 25C		23.6	-	25.4	ohm	Cpk > 1.33	
III.B.1.b.2	Coil Resistance at -40C		-4	0	+4	%	2/	
III.B.1.b.3	Coil Resistance at +150C		-4	0	+4	%	2/	
III.B.1.c	Dynamic Surge Test		-	P	-	P/F	2/	
III.B.1.d	Pull in voltage (-40°C)		-	-	5.2	V	Cpk > 1.33	
	Pull in voltage (25°C)		-	-	7.8			
	Pull in voltage (150°C)		-	-	18.4			
III.B.1.e	Release voltage		50	300	-	mV	2/	
III.B.1.f	Clutch Clamping Force		89.0	104.0	-	N	Cpk > 1.33	
III.B.1.g	Output Gear		-	P	-	P/F	2/	
III.B.1.h	Bobbin		-	P	-	P/F	2/	
III.B.2	Servo Functional Tests	PV/IP						6/shift/line
III.B.2.a	Antibacklash Gear		-	P	-	P/F	2/	
III.B.2.b	Electrical Isolation		50	-	-	Mohm	1/	
III.B.2.c.1	Phase Resistance at 25C		2.30	2.65	2.81	ohm	Cpk > 1.33	
III.B.2.c.2	Phase Resistance at -40C		-4	0	+4	%	2/	
III.B.2.c.3	Phase Resistance at +150C		-4	0	+4	%	2/	
III.B.2.c.4	Phase - Phase Ohmic Variance		-	0.0	0.11	ohm	Cpk > 1.33	
III.B.2.d	Inductance at 1 khz		7.5	9.5	11.5	mH	Cpk > 1.33	
III.B.2.e	Minimum Pull Voltage		-	-	9.5	V	2/	
III.B.2.f	Maximum Stroke Test		177	178	179	Deg.	2/	
III.B.2.g	No Load Deactivate to Idle		-3.0	0	+3.0	Deg.	2/	
III.B.2.h	Full Load Deactivate to Idle		-3.0	0	+3.0	Deg.	2/	
III.C	Audit tests							
III.C.1	Clutch Tests	PV/IP						10%
III.C.1.a	Pull in voltage				7.0	V	Cpk > 1.33	
III.C.2	Motor/Housing Assembly	PV/IP						10%
III.C.2.a	Inductance at 1 khz.		7.5	9.5	11.5	mH	Cpk > 1.33	
III.C.2.b	Motor Static Torque		23.5	27.0	30.6	oz-in	Cpk > 1.33	5/hr
III.C.2.c	Motor Dynamic Torque		16.0		21.6	oz-in	1/	5/hr

1/ Capability to be within 3 SIGMA of tolerance limit.
2/ GO/NO-GO type test - all must pass

* It is strongly recommended that ES test sample sizes and frequencies be developed by the manufacturer, with concurrence by the CEMD, and documented in the Control Plan.

PRODUCTION VALIDATION AND IN-PROCESS TESTS
FIGURE 1 - (cont'd)

TEST NUMBER	TEST CHARACTERISTIC	TEST [illegible]	TEST LIMITS OVER SPECIFIED TEMPERATURE				MINIMUM CONFORMANCE TO TOLERANCE	SUGGESTED* SAMPLE SIZE /FREQUENCY
			MIN	TARGET	MAX			
III.D	100% In-process Tests							
III.D.1	Clutch Tests	PV/IP						100%
III.D.1.a	Dielectric Test		-	-	95	mA	2/	
III.D.1.b	Dynamic Surge Test		-	P	-		2/	
III.D.1.c	Pull in voltage		-	-	7.0	V	2/	
III.D.1.d	Release voltage		140	-	-	mV	2/	
III.D.1.e	Output Gear		-	P	-	P/F	2/	
III.D.2	Stator	PV/IP						100%
III.D.2.a	Hi Pot		-	1000	-	Volts	2/	100%
III.D.2.b.1	Phase Resistance		2.3	2.55	2.81	ohm	2/	100%
III.D.2.b.2	Phase - Phase Ohmic Variance		-	-	0.11	ohm	2/	
III.D.2.c	Dynamic Surge Test		-	P	-	P/F	2/	
III.D.3	Motor/Housing Assembly	PV/IP						100%
III.D.3.a	Inductance at 1 khz		7.5	-	11.5	mH	2/	
III.D.3.b	Motor Static Torque		23.5	27.0	30.5	oz-in	1/	5/hr
III.D.3.c	Dielectric Test		-	-	1.0	mA	2/	
III.D.4.	Actuator Assembly	PV/IP	-4	0	+4	%	2/	100%
	End of Line Tests						2/	
III.D.4.a	Electrical Isolation		5	-	-	Mohm	1/	5/hr
III.D.4.c	Minimum Pull Voltage		-		9.5	V	2/	
III.D.4.d	Maximum Stroke Test		177	178	179	Deg.	2/	
III.D.4.e	No Load Deactivate to Idle		-3.0	0	+3.0	Deg.	2/	
III.D.4.f	Full Load Deactivate to Idle		-3.0	0	+3.0	Deg.	2/	
III.D.4.h	Rotor Rub Test		-	4.0	-	V	2/	
III.E	Durability Tests							
	Lot Control							
III.E.1	6 Hour Accelerated life test	PV/IP	-	P	-	P/F	2/	6/shift/wk
	Audit							
III.E.2	Humidity Test	PV/IP	-	P	-	P/F	2/	3 pcs 2x/Mo
III.E.3	Phase Resistance		2.30	2.55	2.81	ohm	Cpk > 1.33	

1/ Capability to be within 3 SIGMA of tolerance limit.
2/ GO/NO-GO type test - all must pass

* It is strongly recommended that ES test sample sizes and frequencies be developed by the manufacturer, with concurrence by the CSMO, and documented in the Control Plan.

3 TEST PROCEDURES AND REQUIREMENTS

A. General

Every Speed Control Servo assembly or subassembly shall be capable of passing the Functional, Production Validation, In-Process and End of Line Test specified. Factory ambient tests shall be conducted at 25°C ± 8°C. In addition to all the tests specified herein, all actuator assemblies F2VF-9A819, must meet the Speed Control Actuator final assembly (electronics installed) specification ES-F2VF-9C735-AA

B. Functional Tests

Three Temperature Functional (-40°C, 25°C, 150°C)

Unless otherwise specified, assemblies must meet this specification in the temperature range of -40°C to 150°C. Sample testing must be performed at -40°C, 25°C, and 150°C ambient. Unless the procedure itemized below is used, the environmental chamber soak time when performing functional tests at temperature extremes shall be 2 hours. This allows the servo to stabilize at the final test temperature for most chamber capacities and loading. The limiting factor being the chamber cooling capacity when fully loaded.

The soak time in the QC audit area may be reduced for three temperature functional testing if the time required to reach the temperature extremes, both hot and cold, is determined using a thermocouple type thermometer and a thermocoupled sample module. Procedure:

- Prepare a test sample module by drilling and tapping a #6-32 thread in an area of the module casting having the thickest cross section next to the motor. (This test sample should be saved for future use.)
- Using a #6-32 screw and washer, clamp a thermocouple under the washer firm against the module. (Alternate methods for attachment are not permitted).
- Load the chamber with the necessary fixtures, the maximum number of modules to be tested including the temperature verification module having the threaded hole in the casting and the thermocouple clamped using a screw and washer. Be sure the module containing the thermocouple is mounted at the station closest to the door.
- Record the time required for the verification module to stabilize within 2 degrees of final value.
- Take the stabilization times for hot and cold and adjust by multiplying each by 1.1 to account for unknown factors that will occur during normal testing.
- Use the adjusted time as the soak requirement. Post the soak time and date of validation and date of next revalidation on the front of the test equipment. Submit the adjusted soak times to CEMO.

The chamber soak time must be revalidated as follows:

- Every 6 months
- If any chamber service is done to correct a chamber problem,
- If the thermal loading of the chamber is increased (more things added to chamber since the last time Validated),
- If a different chamber is used.

3 TEST PROCEDURES AND REQUIREMENTS (cont'd)

B. Functional Tests (cont'd)

1. Clutch Subassembly Functional Test (reference Figure 3)

Passive tests (-40°C, 25°C and 150°C)
Use an external clamp to close the clutch so the drive teeth are meshed together resulting in the minimum air gap and verify these electrical parameters.

a. Dielectric test (25°C Only)
This test is designed to measure dielectric strength of the clutch and is sometimes referred as a "HIPOT" test.

Make an electrical connection across one lead of the clutch and the clutch shaft. Apply 1500 volts, 60 Hz a.c. to the connection and measure the resultant current flow. The high voltage stimulus is not to exceed a duration of 1 second.

b. Coil Resistance
The measurement method below verifies the integrity of the part at three temperatures as well as the sample temperature when the data is collected. If the test sample is defective or the test temperature is incorrect, the result will be out of specified limits.

1. With the coil at 25°C, measure and record the resistance.

2. With the coil temperature at -40°C, calculate the test result using:

$$\text{Result} = \frac{(R\text{-}40°C \times 1.334 - R25°C)}{(R25°C)} \times 100$$

Where:

1) R-40°C is the coil resistance measurement at -40°C
2) R25°C is the resistance value recorded at test III.B.1.b.1

3. With the coil temperature at 150°C, calculate the test result using:

$$\text{Result} = \frac{(R150°C \times 0.675 - R25°C)}{(R25°C)} \times 100$$

Where:

1) R150°C is the coil resistance measurement at 150°C
2) R25°C is the resistance value recorded at test III.B.1.b.1

3 TEST PROCEDURES AND REQUIREMENTS (cont'd)

B. Functional Tests (cont'd)

1. Clutch Subassembly Functional Test (cont'd)

c. Dynamic Surge Test (25°C Only)
Use a Slaughter Co. Model 1648-1.5 Dynamic Surge Tester for this test. This test verifies consistency in the device magnetics and is most sensitive to detection of shorted turns. It is a GO/NO-GO type test calibrated using GO/NO-GO masters.

Gage Masters
The GO and the NO-GO calibration masters are to be verified as dimensionally correct. The GO master is to be verified magnetically and electrically correct using a high voltage RF inductance meter. The NO-GO master shall be constructed to contain 30 shorted turns. The specific details for construction of these masters is the responsibility of the supplier and documentation to be available to Ford ELD upon request.

Calibration
Calibrate the Slaughter Model 360 using the provided Phase and Balance controls to consistently pass the GO master and reject the NO-GO master. The transient wave form of the GO master is to be digitally stored in the tester memory for use during the normal test cycle. The tester reject limits must be verified to consistently reject a part containing 30 shorted turns.

Stimulus
Stimulate the part under test using a single 500 volt, 1 millisecond impulse. The test equipment will automatically compare the tested part transient wave form to the digitally stored wave form produced by the "GO" master during calibration. The deviation in the wave form shall be less than the "NO-GO" master containing 30 shorted turns.

Active Tests (-40°C, 25°C and 150°C)

d. Pull in voltage
Apply a voltage to the clutch terminal contacts at a rate of 0.5 volts per second and record the voltage the clutch engages.

e. Release voltage

1. To initialize the clutch magnetics, energize the coil to 16.0 ± .1 volts and verify the output gear engages with the pole piece face teeth and is fully clamped.

2. With the face teeth fully engaged, reduce the voltage to 50 ± 1 mV, the clutch must release within 250mS

f. Clutch Clamping Force (Performed at Factory Ambient Temperature Only)

1. Energize the clutch coil to 287 ± 1 ma and verify the output gear engages with the pole piece face teeth and is fully clamped.

2. Apply an external force to the rim of the output gear. Record the peak force required to separate the output gear from the pole piece.

3 TEST PROCEDURES AND REQUIREMENTS (cont'd)
B. Functional Test (cont'd)
1. Clutch Subassembly Functional Test (cont'd)

Free Motion Tests (performed at -40°, 25° and 150°C)
The clutch assembly contains three parts which must demonstrate free relative motion. These are the output gear, coil bobbin, and shaft/pole piece.

g. Output Gear
When de-energized, the output gear must freely rotate 360 degrees relative to the output shaft.

h. Bobbin
The bobbin connector, relative to the shaft flat, must freely rotate 190 degrees with the clutch energized to 18 volts.

2. Servo Three Temperature Functional Tests (-40°C, 25°C, 150°C)

Passive tests
a. Antibacklash Gear (Performed at Factory Ambient Temperature Only)
Antibacklash gear bias springs are to be checked for correct installation.

b. Electrical Isolation (25°C Only)
Electrical isolation from phases to shaft to be checked at 500 volts DC.

c. Phase Resistance.
The measurement method below verifies the integrity of the part at three temperatures and well as the sample temperature when the data is collected. If the test sample is defective or the test temperature is incorrect, the result will be out of specified limits.

1. With the motor at 25°C, measure and record the resistance of phase A.

2. With the motor temperature at -40°C, calculate the phase A test result using:

$$\text{Result} = \frac{(R{-40}^\circ C \times 1.334 - R25^\circ C)}{(R25^\circ C)} \times 100$$

Where:

1)R-40°C is the phase resistance measurement at -40°C2

2)R25°C is the resistance value recorded at test III.B.2.c.1.

3. With the motor temperature at 150°C, calculate the Phase A test result using:

$$\text{Result} = \frac{(R150^\circ C \times 0.675 - R25^\circ C)}{(R25^\circ C)} \times 100$$

Where:

1)R150°C is the phase resistance measurement at 150°C

2)R25°C is the resistance value recorded at test III.B.2.c.1.

Repeat for phases B and C.

4. Check the phase to phase resistance variance.

3 TEST PROCEDURES AND REQUIREMENTS (cont'd)

B. Functional Test (cont'd)

2. Servo Three Temperature Functional Tests (cont'd)

d. Inductance at 1 kHz (Series Method)(25°C only)
Align the motor shaft in the phase A detent position and measure phase A inductance. Repeat for phases B and C.

Three Temperature Active Tests (-40°C, 25°C, 150°C):
Setup the gearbox assembly with output shaft position sensor and load as shown in figure 4 and perform the following set of tests. Be sure an axial load of 22± 2N is transferred to the actuator output pully per figure 4, all motor stepping sequences are executed exactly per Figures 6A & 6B and the power drive suppression circuits are the same as shown in Figure 5.

e. Minimum Pull Voltage:
1. With the actuator output shaft unloaded and clutch disengaged, save the shaft angular position for use in the "No Load deactivate to Idle" test III.B.2.g.

2. Apply a load to the actuator as shown in Figure 7, keep the clutch disengaged, and save the output shaft position for use in test III.B.2.e.9.

3. Power up the clutch using a constant current source set for 287 ± 1 ma and dwell 150ms minimum to allow time for the clutch to close.

4. Set the motor supply voltage to 14 ± 0.1 volts.

5. To pickup the load and minimize all lash within the actuator assembly and test equipment, advance the output shaft angle making an initial move of 50 motor steps per starting/stopping phase stepping sequences of Figures 6A and B. Save the output shaft angle for use in test III.B.2.e.9.

6. Reduce the motor supply voltage to 9.5 ± .05 volts.

7. Advance the motor shaft 50 steps per starting/stopping phase stepping sequences of Figures 6A and B.

8. Measure the angular rotation of the loaded output shaft. To verify there were no step errors, for each 50 steps, the angle of rotation must be 18.65° ± 0.75°.

f. Maximum Stroke Test:
Continuing from the "Minimum Pull Voltage" test III.B.2.e.9, return the motor supply to 14 ± 0.1 volts and verify the maximum allowable angular displacement from the idle position is attainable. The shaft angle measurement is to be referenced to the saved reading in test step III.B.2.e.2. The steps required to achieve full stroke should be calculated. It is not intended that the actuator be driven into the internal high end hard stop by the motor. Calculate the required number of steps using:

3 TEST PROCEDURES AND REQUIREMENTS (cont'd)

B. Functional Test (cont'd)

2. Servo Three Temperature Functional Tests (cont'd)

Three Temperature Active Tests (-40°C, 25°C, 160°C):

f. Maximum Stroke Test (cont'd)

$$\text{Steps Needed} = \left(\text{Upper Spec. limit} - \text{Total angle from III.B.2.e.9} \right) \times 5.691$$

g. No Load Deactivate to Idle:

Continuing from the "Maximum Stroke" test III.B.2.f, remove the load from the actuator.

Remove power from the motor and clutch and verify the internal actuator return spring moves the output to the idle position saved in test III.B.2.e.1.

h. Full Load Deactivate to Idle:

1. Power up the clutch using a constant current source set for 287 ± 1 ma and dwell 150ms minimum to allow time for the clutch to close.

2. Apply a load to the gearbox as shown in Figure 7 and save the shaft position of the actuator with the output shaft loaded and clutch disengaged for use in test III.B.2.h.4.

3. Advance the motor shaft 74 steps per starting/stopping phase stepping sequences of Figures 6A and B. Check for the actuator to advance a minimum of 13°.

4. Reduce the clutch current to 15 ± 1ma and check for the actuator to return to the idle position. Measure and record this position referenced to the reading of test III.B.2.h.2.

3 TEST PROCEDURES AND REQUIREMENTS (cont'd)

C. Audit Tests

1. Clutch Subassembly Audit Test (reference Figure 3)
(Performed at Factory Ambient Temperature)

a. Pull in voltage

Apply a voltage to the clutch terminal contacts at a rate of 0.5 volts per second and record the voltage the clutch engages.

2. Motor/Housing Assembly Audit Tests
(Performed at Factory Ambient Temperature)

a. Inductance at 1 khz (Set Inductance Meter for Series Connection)

Align the motor shaft in the phase A detent position and measure the phase A inductance. Repeat for phases B and C.

b. Motor Static Torque

Apply 2 + 0.05 amps to phase A. Measure and record the peak torque developed at the motor shaft. Repeat for Phases B and C.

c. Motor Dynamic Torque

This test certifies the motor dynamic torque as assembled in the housing. Because the developed motor torque is dependant on motor speed and drive circuit, the motor stepping sequences are to be executed exactly per Figures 6A and the power drive suppression circuits are the same as shown in Figure 5.

With reference to Figures 5 and 6A, use a supply voltage of 13 ± 0.1 volts. Step the motor at constant speed as indicated in figure 6A and apply a torque load to the motor output shaft. Measure the pull out torque by increasing the torque load until a stepping error occurs. Record the developed pull out torque.

3 TEST PROCEDURES AND REQUIREMENTS (cont'd)

D. In-Process Tests (Performed at 22°C))

1. Clutch In-Process Tests (cont'd)

a. Dielectric test
This test is designed to measure dielectric strength of the clutch and is sometimes referred as a "HIPOT" test.

Make an electrical connection across one lead of the clutch and the clutch shaft. Apply 1500 volts, 60 Hz a.c. to the connection and measure the resultant current flow. The high voltage stimulus is not to exceed a duration of 1 second.

b. Dynamic Surge Test
Use a Slaughter Co. Model 1640-1.5 Dynamic Surge Tester for this test. This test verifies consistency in the device magnetics and is most sensitive to detection of shorted turns. It is a GO/NO-GO type test calibrated using GO/NO-GO masters.

Gage Masters
The GO and the NO-GO calibration masters are to be verified as dimensionally correct. The GO master is to be verified magnetically and electrically correct using a high voltage RF inductance meter. The NO-GO master shall be constructed to contain 30 shorted turns. The specific details for construction of these masters is the responsibility of the supplier and documentation to be available to Ford ELD upon request.

Calibration
Calibrate the Slaughter Model 360 using the provided Phase and Balance controls to consistently pass the GO master and reject the NO-GO master. The transient wave form of the GO master is to be digitally stored in the tester memory for use during the normal test cycle. The tester reject limits must be verified to consistently reject a part containing 30 shorted turns.

Stimulus
Stimulate the part under test using a single 500 volt, 1 millisecond impulse. The test equipment will automatically compare the tested part transient wave form to the digitally stored wave form produced by the "GO" master during calibration. The deviation in the wave form shall be less than the "NO-GO" master containing 30 shorted turns.

Active Tests.

c. Pull in Voltage
Apply 7 ± 0.1 volts DC and verify the clutch engages.

d. Release voltage
1. To initialize the clutch magnetics, energize the coil to 16.0 +/- .1 volts and verify the output gear engages with the pole piece face teeth and is fully clamped.

2. With the face teeth fully engaged, reduce the voltage to 140 ±1 mV, the clutch must release instantly

3 TEST PROCEDURES AND REQUIREMENTS (cont'd)

D. In-Process Tests (cont'd)

1. Clutch In Process Tests (cont'd)

Free Motion Tests
The clutch assembly contains three parts which must demonstrate free relative motion. These are the output gear, coil bobbin, and shaft/pole piece.

e. Output Gear
When de-energized, the output gear must freely rotate 360 degrees relative to the output shaft.

2. Stator (Performed at Factory Ambient Temperature)

a. Electrical Isolation
Hi Pot test at 1000 VAC and 95 mA for one second duration

b. Phase Resistance
1. Resistance value to be checked for each of the three phases.

2. Check the phase to phase resistance variance.

c. Dynamic Surge Test
Use a Slaughter Co. Model 1648-1.5 Dynamic Surge Tester for this test. This test verifies consistency in the device magnetics and is most sensitive to detection of shorted turns. It is a GO/NO-GO type test calibrated using GO/NO-GO masters.

Gage Masters
The GO and the NO-GO calibration masters are to be verified as dimensionally correct. The twelve poles of the stator are to be connected electrically into a single series connection. The GO master is to be verified magnetically and electrically correct using a high voltage RF inductance meter. The NO-GO master shall be constructed to contain 6 (six) shorted turns. The specific details for construction of these masters is the responsibility of the supplier and documentation to be available to Ford ELD upon request.

Calibration
Calibrate the Slaughter Model 360 using the provided Phase and Balance controls to consistently pass the GO master and reject the NO-GO master. The transient wave form of the GO master is to be digitally stored in the tester memory for use during the normal test cycle. The tester reject limits must be verified to consistently reject a part containing 6 (six) shorted turns.

Stimulus
The twelve poles of the stator are to be connected electrically into a single series connection. Stimulate the part under test using a single 500 volt, 1 millisecond impulse. The test equipment will automatically compare the tested part transient wave form to the digitally stored wave form produced by the "GO" master during calibration. The deviation in the wave form shall be less than the "NO-GO" master containing 6 (six) shorted turns.

3 TEST PROCEDURES AND REQUIREMENTS (cont'd)

D. In-Process Tests (cont'd)

3. Motor/Housing Assembly (Performed at Factory Ambient Temperature)

a. Inductance at 1 kHz (Series Method)
Align the motor shaft in the phase A detent position and measure the phase A inductance. Repeat for phases B and C.

b. Motor Static Torque
Apply 2 + 0.05 amps to phase A. Measure and record the peak torque developed at the motor shaft. Repeat for Phases B and C.

c. Dielectric Test
This test is designed to check the dielectric strength of the motor stator windings and is sometimes referred to as a "HIPOT" test.

Make an electrical connection to the motor windings and the motor housing. Apply 600 volts AC for a period of 1 second.

4. Actuator Assembly End of Line Tests
(Performed at Factory Ambient Temperature)

Passive tests

a. Electrical Isolation

Electrical isolation from phases to shaft to be checked at 500 volts DC.

End Of Line Active Tests:

Setup the gearbox assembly with output shaft position sensor and load as shown in figure 4 and perform the following set of tests. Be sure an axial load of 22 + 2N is transferred to the actuator output pully per figure 4, all motor stepping sequences are executed exactly per Figures 6A & 6B and the power drive suppression circuits are the same as shown in Figure 5.

b. Minimum Pull Voltage:

1. With the actuator output shaft unloaded and clutch disengaged, save the shaft angular position for use in the "No Load deactivate to Idle" test III.D.4.e.

2. Apply a load to the actuator as shown in Figure 7, keep the clutch disengaged, and save the output shaft position for use in test III.D.4.c.9.

3. Power up the clutch using a constant current source set for 287 ±1 ma and dwell 150ms minimum to allow time for the clutch to close.

4. Set the motor supply voltage to 14 ± 0.1 volts.

3 TEST PROCEDURES AND REQUIREMENTS (cont'd)

D. In-Process Tests (cont'd)

4. Actuator Assembly End of Line Tests (cont'd)

End Of Line Active Tests: (cont'd)

b. Minimum Pull Voltage:

5. To pickup the load and minimize all lash within the actuator assembly and test equipment, advance the output shaft angle making an initial move of 50 motor steps per starting/stopping phase stepping sequences of Figures 6A and B. Save the output shaft angle for use in test III.D.4.c.8.

6. Reduce the motor supply voltage to 9.5 ± .05 volts.

7. Advance the motor shaft 50 steps per starting/stopping phase stepping sequences of Figures 6A and B.

8. Measure the angular rotation of the loaded output shaft. To verify there were no step errors, for each 50 steps, the angle of rotation must be 18.65 ± 0.75°.

c. Maximum Stroke Test:

Continuing from the "Minimum Pull Voltage" test III.D.4.c.9, return the motor supply to 14 ± 0.1 volts and verify the maximum allowable angular displacement from the idle position is attainable. The shaft angle measurement is to be referenced to the saved reading in test step III.D.4.e.2. The steps required to achieve full stroke should be calculated. It is not intended that the actuator be driven into the internal high end hard stop by the motor. Calculate the required number of steps using:

$$\text{Steps Needed} = \left(\text{Upper Spec. limit} - \text{Total angle from III.D.4.c.9} \right) \times 2.681$$

d. No Load Deactivate to Idle:

Continuing from the "Maximum Stroke" test III.D.2.d, remove the load from the actuator.

Remove power from the motor and clutch and verify the internal actuator return spring moves the output to the idle position saved in test III.D.4.c.1.

3718 7240

3 TEST PROCEDURES AND REQUIREMENTS (cont'd)

D. In-Process Tests (cont'd)

4. Actuator Assembly End of Line Tests (cont'd)

End Of Line Active Tests: (cont'd)

e. Full Load Deactivate to Idle:

1. Power up the clutch using a constant current source set for 287 ± 1 ma and dwell 150ms minimum to allow time for the clutch to close.

2. Apply a load to the gearbox as shown in Figure 7 and save the shaft position of the actuator with the output shaft loaded and clutch disengaged for use in test III.D.2.f.4.

3. Advance the motor shaft 74 steps per starting/stopping phase stepping sequences of Figures 6A and B. Check for the actuator to advance a minimum of 13°.

4. Reduce the clutch current to 15 ± 1ma and check for the actuator to return to the idle position. Measure and record this position referenced to the reading of test III.D.2.f.2.

f. Rotor Rub Test

Engage clutch at 7.0 ± 0.1 volts. Step the motor at 240 steps per second using specified voltage into driver card & no current limiting. Step the motor for 1.7 seconds clockwise and then turn clutch voltage supply to 150 mv. Step the motor for 1.3 seconds counter-clockwise. The rotor must rotate freely in both directions with no binding or resonances (pauses or jerky motion) and the clutch must return to the rest position.

3 TEST PROCEDURES AND REQUIREMENTS (cont'd)

E. Durability Tests

Unless otherwise specified, the Speed Control assembly shall pass section III.B after sustaining any of the following durability tests. Under no circumstances shall a Speed Control unit, subjected to any of these durability tests, be shipped for vehicle installation.

1. 6 Hour Accelerated Life Test

The purpose of the test is to identify any supplier/process defects before shipment of a lot. The test will cause servo wear out shortly after the 6 hour test cycle but not before 5 hours. The wear out should occur in various forms indicating the stress on the different components is balanced. The test cycle and fixture is determined by the supplier. For reference, use the accelerated test fixture shown in Figure 8 and the load applied to the Servo assembly depicted in Figure 7. The test cycle of Table 1 is for reference.

2. Humidity Test

Expose the Servo to 85°C and 85% relative humidity for 96 Hours. Immediately after removal from the test chamber, the Servo must pass performance test per III.B.2 at 25°C only.

3. Phase Resistance

Resistance value to be checked for each of the three phases.

4 REVALIDATION REQUIREMENTS

The manufacturing source and the design-responsible Component Engineering and Manufacturing Operations will jointly determine which potential changes to the process, materials or material sources would have significant impact on the product's function, performance, durability or appearance. The supplier will describe these conditions in the Control Plan, along with either

(1) the revalidation plan that would be followed in each case, or
(2) a provision to submit an amended Control Plan for approval if any of those process changes are planned.

The Control Plan must include a provision that, for any significant change in processing, ELD-CEMO and the manufacturing location (internal or supplier) shall jointly determine if PV re-testing is required, and, if so, to what degree, i.e., Full or Mini-PV.

No change to processing may be allowed without prior engineering approval of the process changes and the attendant Control Plan changes.

5 INSTRUCTIONS AND NOTES

A. Control Plans

Control Plans address all significant design and process characteristics, which include all ES tests and Control Item characteristics. They describe the process potential studies that will be performed for product validation (including PV tests) and the ongoing product and process evaluation for continuing improvement (including IP tests). They include acceptance criteria, sample sizes, frequencies, data analysis methods and reaction plans.

The Control Plan is developed, and updated as necessary, by the manufacturing source in conjunction with the design responsible Component Engineering and Manufacturing Operations and other appropriate functions such as STA. The Control Plan defines the management of the upstream production process and part variables (significant process characteristics) that affect the outcome of the ES tests or other significant design characteristics. The Control Plan also identifies the specific ES tests, with their sample sizes and frequencies, that will be performed in order to:

1. Confirm whether the process is being managed effectively.
2. Further identify significant process characteristics.
3. Evaluate performance of marginal processes.
4. Better anticipate the customer effect of proposed process improvements.

For any part on which ES tests have been specified, the manufacturing source must present the Control Plan and any revisions to the design responsible Product Design Office for approval. This Component Engineering and Manufacturing Operations has flexibility to honor business relationships with suppliers having proprietary processes.

B. Lot Definition

A lot consists of no more than one shift of production. The size of the lot does not affect the minimum sample size. The audit sample sizes are not to be reduced due to short production runs even though 100 percent inspection results.

5 INSTRUCTIONS AND NOTES (cont'd)

C. Test Reporting and Record Retention

Recording and record retention shall conform to Ford QS-9000 Section 4.2. In addition:

1. Production Validation

All PV samples and the test results and data from Production Validation testing must be submitted in report form to ELO-CEMO prior to PSW. Component Engineering and Manufacturing Operations shall have final authority to approve PV testing.

2. In-Process

The IP test variable data produced as a result of performing the sample lot test requirements outlined in Section II must be collected and stored as defined in QS-9000 for ELO-STA review.

3. Report Contents for Lot Control Testing

Equipment serial numbers, most recent date of calibration and test sample serial number must be recorded on all data sheets Test summaries must be sorted by test temperatures -40°C, 25°C, 150°C or 170°C, and contain:

1) Sample Size
2) X - BAR
3) High Reading
4) Low Reading
5) Standard Deviation
6) Cp and Cpk
7) Upper Test Limit
8) Lower Test Limit

The records must be stored such that all parametric data for any one sample piece may be recalled with traceability to the lot in which the sample was taken.

D. Test Correlation

Test equipment correlation between on-line and audit test equipment shall be performed by supplier. The procedure must be documented in the supplier control document.

E. Returns - ELO/Body & Assembly Division/Field

The supplier shall have the capability to analyze all returns and shall identify the root cause of the returns. A report for each identified root cause is to be delivered to ELO-CEMO on a timely basis. All test methods and data used to identify the root cause will be submitted together with a report in an 8D format. Summary data of these results must be provided to ELO-CEMO monthly. Destructive analysis not allowed without prior approval from ELO-CEMO.

5 INSTRUCTIONS AND NOTES (cont'd)

F. Traceability

The manufacturer shall institute a traceability program per Visteon QS-9000 3.14 for all components:

Bearings, shafts, housings, gears, wire, molded parts, retainers, connector inserts, pole pieces, adhesives, stampings, clips, springs.

In addition, each time a module is subjected to any of the daily IP Sample Tests 3.5, the test number, test results, (parametric data), and date tested shall be traceable from the clearly and permanently marked assembly.

G. Repairs

1. Definition
A repair is defined as the rework required for a module to pass a test requirement.

2. Procedure
Repair of the modules may not be done until the manufacturers repair procedure is approved by ELD-CEMO.

VI. COMPILATION OF REFERENCE DOCUMENTS

ES-F2VF-9A819-AA HOUSING ASY-SPEED CONTROL ACTU
ES-F2VF-9C735-AA SERVO ASSEMBLY SPEED CONTROL
ES-F2VF-9D844-AA AMPLIFIER SPECIFICATION
CE-F2VF-9D844-BA AMPLIFIER MONITOR AND MEMORY MAP
ES-F10F-1316-AA ELECTROMAGNETIC COMPATIBILITY CONFORMANCE
QS-9000 1990 VISTEON QUALITY CONTROL
SREA Form #1638, or approved equivalent
FMEA Form #GFD-9368 or approved equivalent
CONTINUING PROCESS CONTROL AND PROCESS CAPABILITY IMPROVEMENT, FMC
VISTEON RELIABILITY METHODS, FMC
PLANNING FOR QUALITY, VISTEON AUTOMOTIVE SYSTEMS
FEP 3-145, SEC. VII, GUIDELINES FOR PART NUMBER IDENTIFICATION ON PARTS

NOTE: Outside suppliers should request all reference information from the Purchasing activity. Where necessary, Purchasing requests these documents from the affected Component Engineering and Manufacturing Operations.

PV TEST FLOW

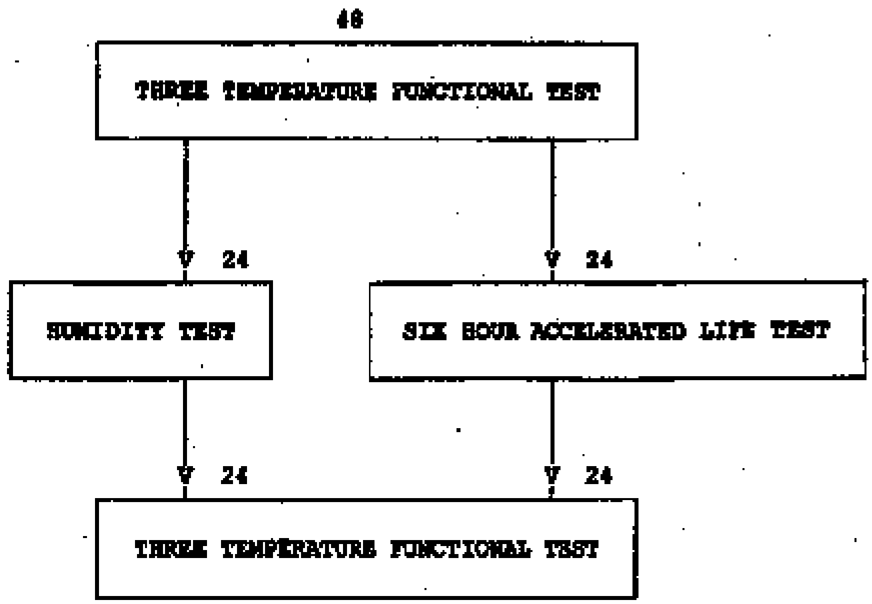


FIGURE 2

CLUTCH TEST SETUP

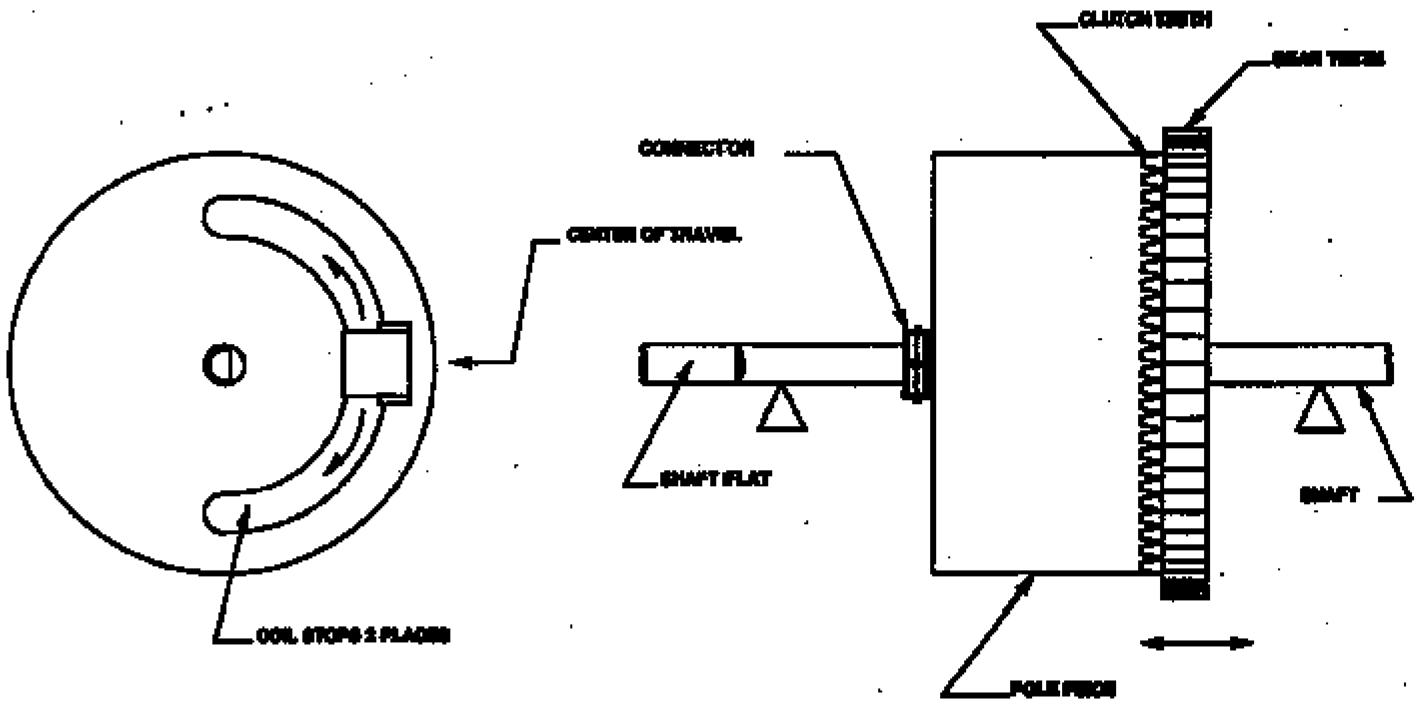


FIGURE 3

FUNCTIONAL TEST FIXTURE

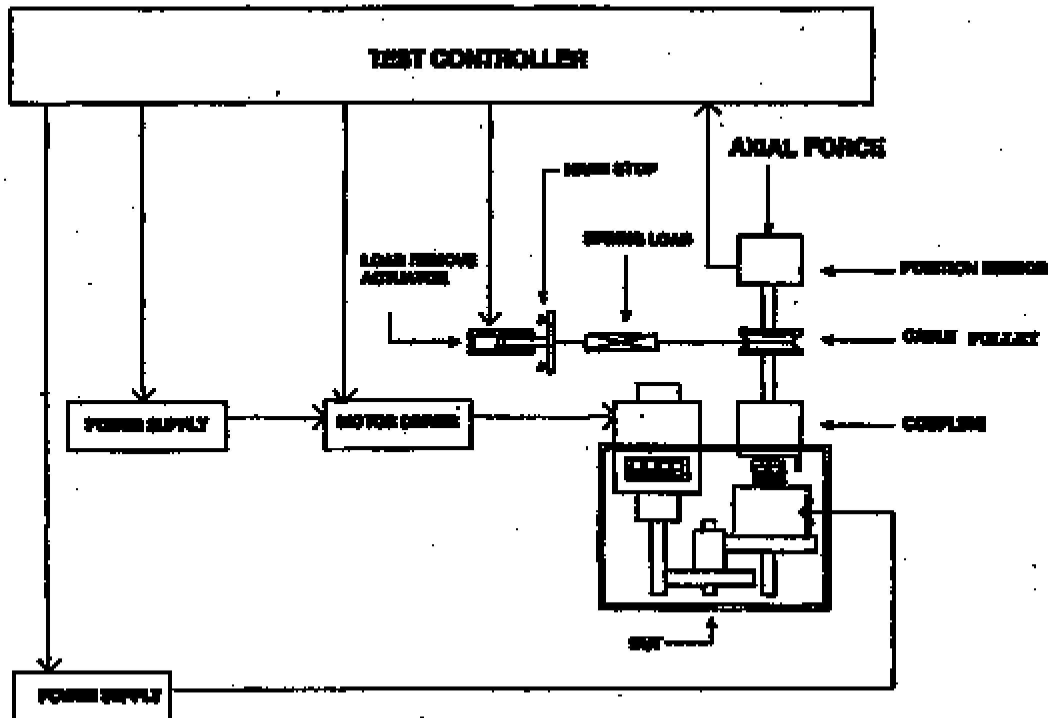


FIGURE 4

FUNCTIONAL TEST DRIVE CURCUIT

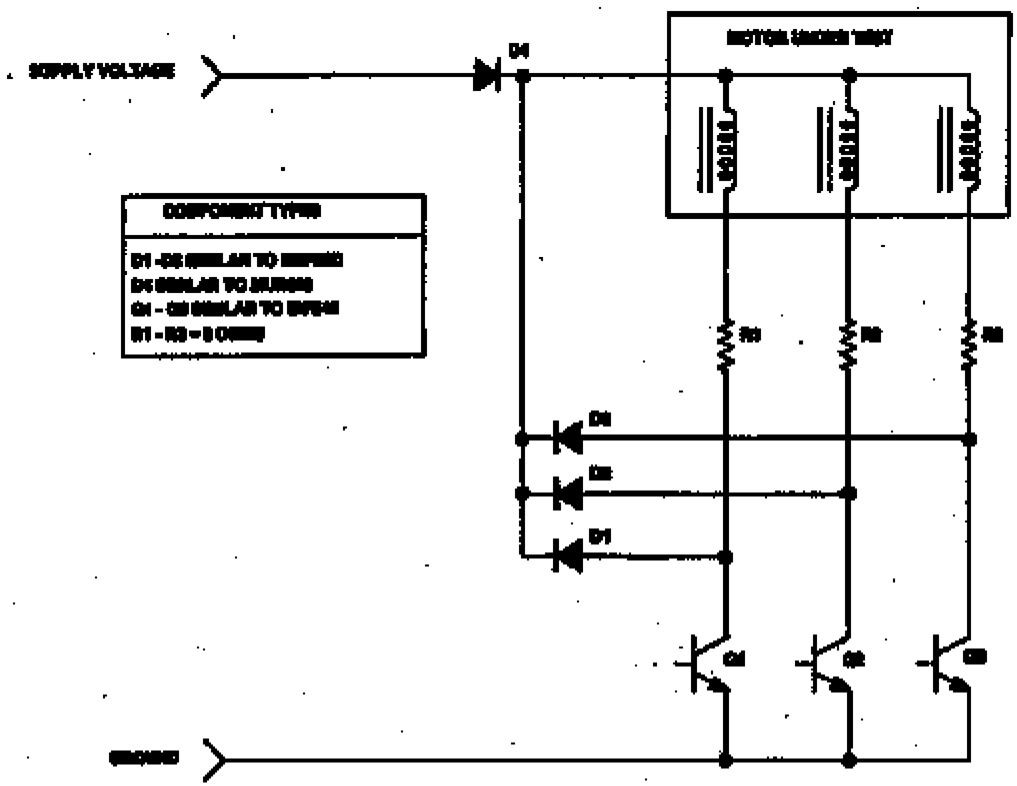
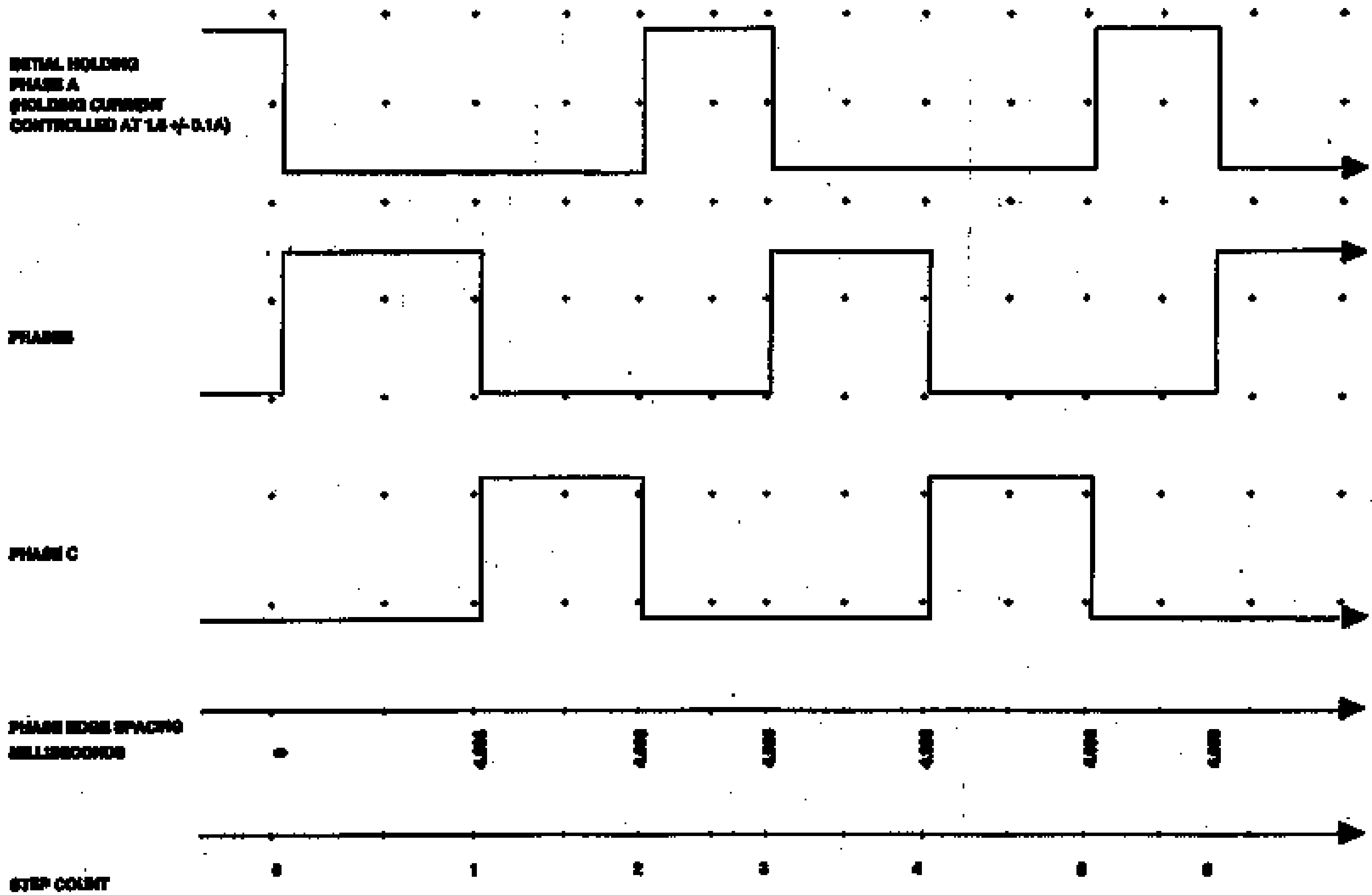
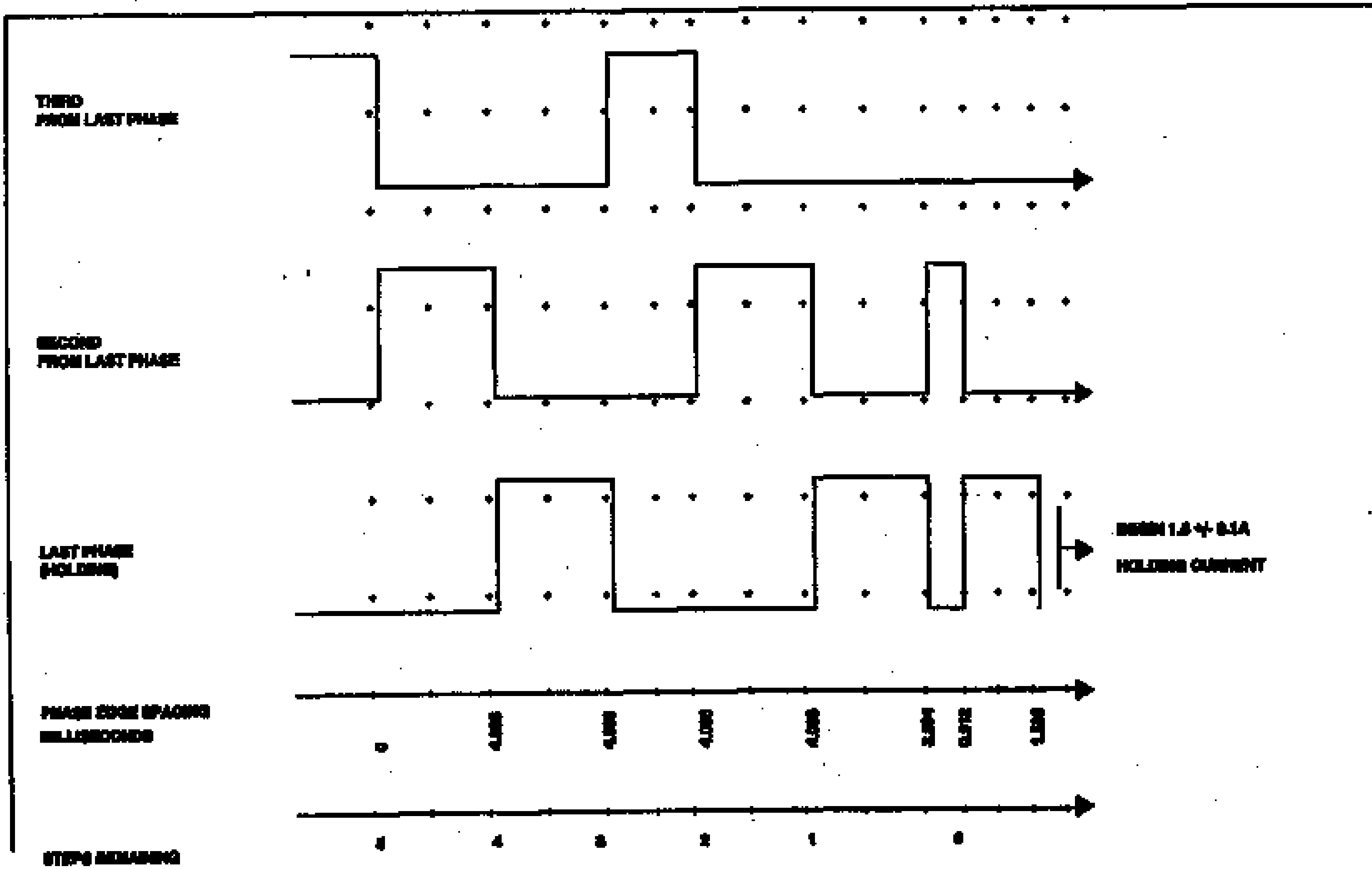


FIGURE 5

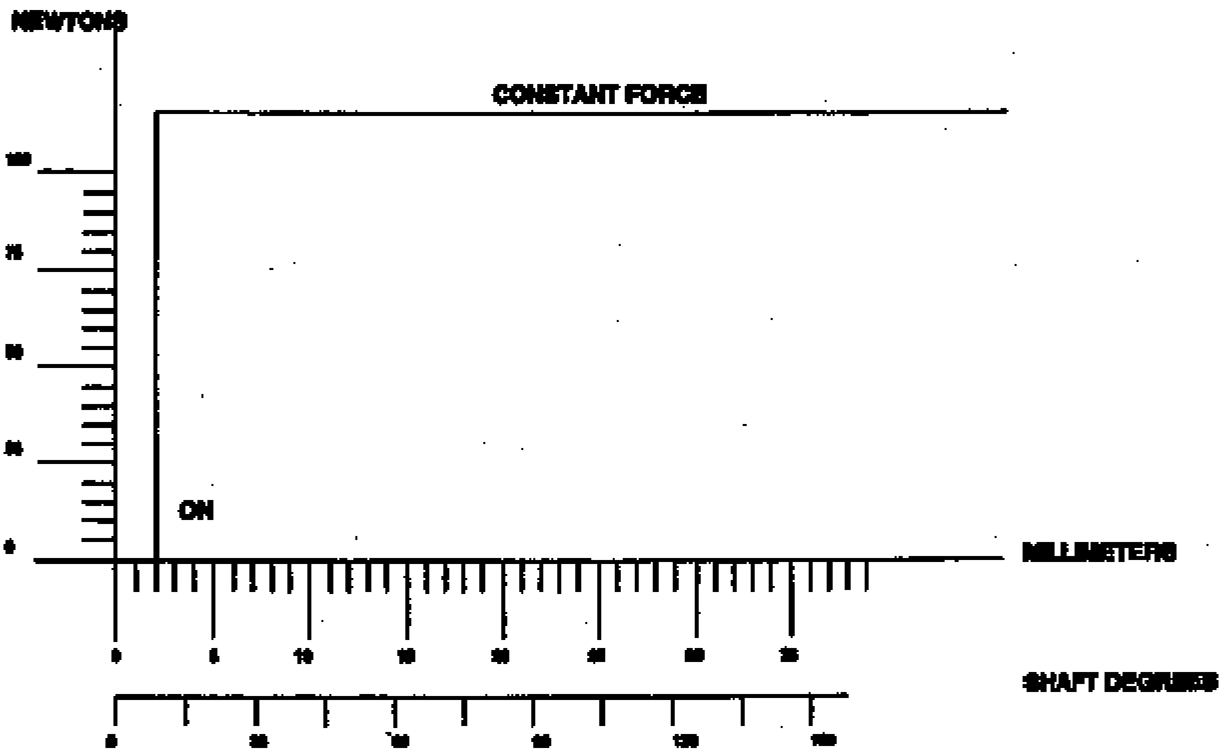


STARTING STEP TIMING
FIGURE 6A



STOPPING STEP TIMING
FIGURE 6B

TEST	FORCE
II.B.2	134 N MIN.
II.D.4	124 N MIN.



LOAD LINE

FIGURE 7

ACCELERATED LIFE TEST FIXTURE

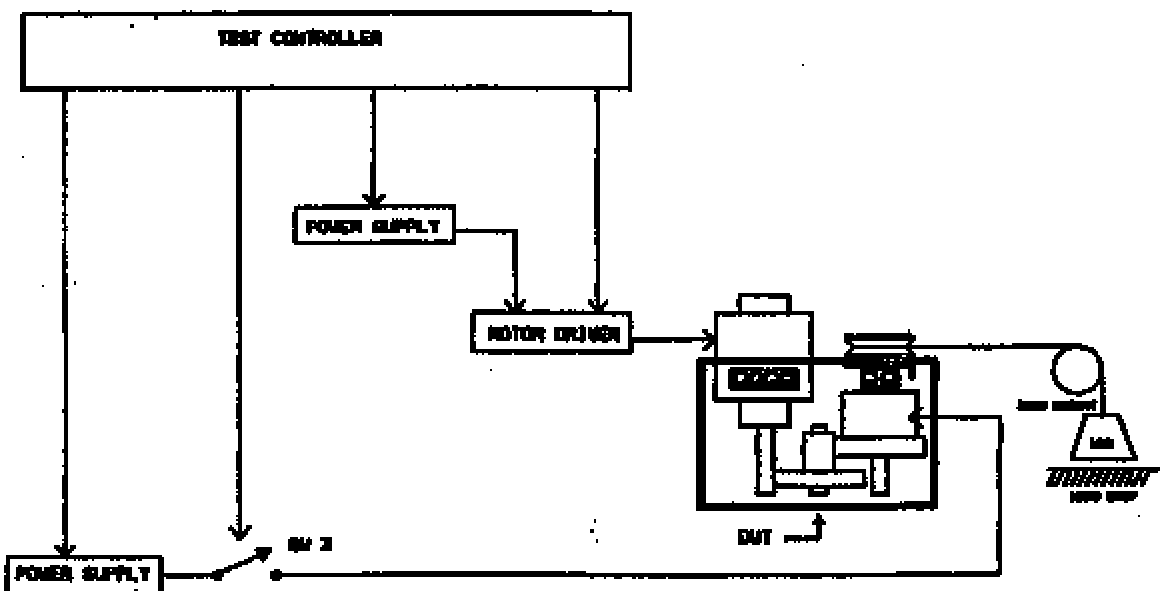


FIGURE 9

Table 1

The accelerated durability test cycle is comprised of segments as indicated below:

- Power up the servo clutch to 500 mA.
- Stroke the servo to W.O.T. (500 steps).
- Stroke the servo toward idle 420 steps and remove the clutch power by opening SW3. This will cause a hard return of the servo against the idle stop of the test fixture.
- Remove power from the module and return to segment "a" of this test cycle.

PART NAME
SPECIFICATION – AMPLIFIER ASSEMBLY – SPEED CONTROL (NEXT GENERATION)

PART NUMBER
ES-F2VF-5D844-AA

LET.		T	T	T	H	N	N	C	C	T	T	T	N	C	C	H	V	[illegible]
FR.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
LET.	W	W	W	N	W	T	T	T	T	T	T	T	D	D	T	T	D	T
FR.	19	20	20A	20C	20D	21	21A	21B	21C	21D	[illegible]	23	24	25	26	27	28	29
LET.																		
FR.	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
LET.																		
FR.	48	49	50	51	52	53												
LET.																		
FR.																		
LET.																		
FR.																		

DATE	LET.	FR.	REVISIONS	DR.	CK.
[illegible]			C. WEBER (313) 84-51455		
[illegible]			PROD REL DE00[illegible]	[illegible]	[illegible]
910701	A	11A	AMP TYPE E/A [illegible] VERSION WAS 11	[illegible]	
			C. WEBER (313) 84-51455		
91[illegible]			DE00[illegible]	[illegible]	[illegible]
	B	11A	AMP TYPE B [illegible] SOFTWARE VERSION		
			WAS 11 & 12		
			C. WEBER (313) 84-51455		[illegible]
910711			DE00[illegible]	[illegible]	[illegible]
	C	52	REVISED RENUMBERED FRAMES		
			C. WEBER (313) 84-51455		
91[illegible]			C[illegible]	[illegible]	[illegible]
	D	[illegible]	REVISED RENUMBERED FRAMES WAS 17	[illegible]	
920301			[illegible] DE00[illegible]		[illegible]
920301			S. [illegible] DE00[illegible]	[illegible]	
	E	18	REV [illegible] FIG 5	[illegible]	
	E	[illegible]	REVISED [illegible]		
	E	[illegible]	REVISED FIG-6		
			[illegible] BROOKS (313) 390-[illegible]		
[illegible]			DE00E [illegible]	[illegible]	[illegible]
	E	[illegible]	REV SECT [illegible]		
	F	18	REV FIG 5		
	F	[illegible]	REV FIG 6		
			TOM SOVITEK (313) [illegible]		
[illegible]			DE00E [illegible]-000	[illegible]	[illegible]
	G	18	REV FIG. 5		
	G	20A	ADDED FIG. 6 "AMP TYPE H"		
	G	22A	ADDED FIG 6 "AMP TYPE H"		
			TOM SOVITEK (313) [illegible]		
[illegible]			DE00E [illegible]-000	[illegible]	[illegible]
	H	[illegible]	REVISED [illegible]		
			TOM SOVITEK (313) [illegible]		
[illegible]			DE00E [illegible]-000	[illegible]	[illegible]
	J	22A	REVISED FIGURE 6		
		22A	TOM SOVITEK (313) [illegible]		
[illegible]			DE00E [illegible]-000	[illegible]	[illegible]
			CONT'D FRAME 14		

NUMBER ES-F2VF-5D844-AA

REV N

FRAME 1 OF 53

FRAME 14 of 53, REV Z

ENGINEERING SPECIFICATION

PART NAME	PART NUMBER
SPECIFICATION - AMPLIFIER ASSEMBLY - SPEED CONTROL (NEXT GENERATION)	[illegible]

LET.	K	K	T			U	N	N	C	C	T	T	T	N	C	C	H	V
PG.	1	1A	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
LET.	T	W	W	[illegible]	[illegible]	T	T	T	T	T	T	T	D	D	T	T	D	T
PG.	18	19	20	[illegible]	[illegible]	21	21A	21B	21C	21D	22	23	24	25	26	27	28	29
LET.																		
PG.																		
LET.																		
PG.																		
LET.																		
PG.																		
LET.																		
PG.																		

DATE	LET.	PG.	REVISIONS	DR.	CK.
	K	18	REV FIG 6		
	K	[illegible]			
	K	22B	REV FIG 6		
			TOM SMUTEK (313) 84-51496		
930218			DECODE 102 58917-000	SV	[illegible]
	L	20	REV FIGURE 6		
			Tom SMUTEK (313)84-51496		
930506			DECODE 102 [illegible]03-000	SV	[illegible]
	M	18	REV FIGURE 5		
	M	20	REV FIGURE 6		
			TOM SMUTEK (313)84-51496		
930616			DECODE 102 [illegible]81-000	SV	[illegible]
	N	2	REV TABLE OF CONTENTS		
	N	5-7	REV FIG 1-3		
	N	13	REV SECT III. A. 2. 3		
			TOM SMUTEK (313)84-51496		
930[illegible]			DECODE 103160135-000	SV	
	P	18	REV FIG-6		
	P	[illegible]	REV FIG-6		
	P	[illegible]	REV FIG-6		
			CURT [illegible] (313)[illegible]		
930[illegible]			DECODE 103[illegible]-000	[illegible]	[illegible]
95[illegible]			DECODE 110305737-000		[illegible]
	Q	17	REV FIG-5	KK	
		20A	REV FIG-6	KK	
		22A	REV FIG-6	KK	
			M. FRIEDRICH (313) 390-[illegible]		
931103			DECODE 10[illegible]-000		[illegible]
	R	2	REV TABLE OF CONTENTS		
	R	10-11	REV SECT III.A.1		
	R	18	REV FIG 5		
	R	20C	REV FIG 6 - ADDED FRAME 20C		
	R	22C	REV FIG 6 - ADDED FRAME 22C		
			MARK FRIEDRICH (313) 39-0[illegible]		
93[illegible]			DECODE 103[illegible]-000	SV	
	T	2	REV TABLE OF CONTENTS		
		3	REV TABLE OF CONTENTS		
		4	UPDATE SECTION II		
		10	REV SECTION III.A.1.B-4		

[illegible]

QUALITY CONTROL/QA

PURCHASING

3718 7257

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Engineering Specification

PART NAME: [illegible]

PART NUMBER: [illegible]

LET			T	T	T	T	U	N	N	C	C	T	T	T	N	C	C	N	V
FR	1	1A	1B	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
LET	T	T	V	V	V	V	V	T	T	T	T	T	T	T	D	D	T	T	D
FR	18	19	20	20A	20B	20C	20D	21	21A	21B	21C	21D	22	23	24	25	26	27	28
LET	T																		
FR	29																		
LET																			
FR																			
LET																			
FR																			
LET																			
FR																			

DATE	LET	FR	REVISIONS	DR	CK
	T	11	REV SECTION [illegible]		
		12	REV SECTION [illegible]		
		18	REV FIGURE 5		
		19	REV FIGURE 6		
		20	REV FIGURE 6		
		20A	REV FIGURE 6		
		20B	REV FIGURE 6		
		20C	ADDITION TO FIGURE 6		
		21	REV FIGURE 6		
		21A	REV FIGURE 6		
		21B	REV FIGURE 6		
		21C	REV FIGURE 6		
		21D	REV FIGURE 6		
		22	ADDITION TO FIGURE 6		
		23	REV FIGURE 7		
		26	UPDATE SECTION [illegible]		
		27	UPDATE SECTION [illegible]		
		29	UPDATE SECTION [illegible]		
			MARK FRIEDRICH (313) [illegible]		
[illegible]			[illegible]	[illegible]	[illegible]
	U	5	REV. FIGURE 1		
	U	17	REV. FIGURE 6		
	U	20A	REV. FIGURE 6		[illegible]
			M. FRIEDRICH (313) [illegible]		
[illegible]			PROD REL [illegible]	[illegible]	
	V	17	REV FIGURE 5		
	V	20	REV FIGURE 6		
	V	20A	REV FIGURE 6		
	V	20C	REV FIGURE 6		
	V	20D	REV FIGURE 6		
			MARK FRIEDRICH (313) [illegible]		
[illegible]			[illegible]	[illegible]	[illegible]
	W	19	REV. FIGURE 6		
	W	20	REV. FIGURE 6		

REFERENCE: C

FRAME 19 OF 53 REV Z

FORM [illegible]

3718 7258

PRODUCED BY FORD

Engineering Specification

PART NAME	PART NUMBER
AMPLIFIER ASSEMBLY - SPEED CONTROL (NEXT GENERATION)	[illegible]

LET	Y	Y	Y	Y										X					
PG	1	1A	1B	1C	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
LET		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y				
PG	16	17	18	19	20	20A	20B	20C	20D	21	21A	21B	21C	21D	22	23	24	25	
LET																			
PG	26	27	28	29															
LET																			
PG																			
LET																			
PG																			
LET																			
PG																			

DATE	LET	PG	REVISIONS	DR	CK	APPROVALS
	W	20A	ADD FIGURE 6			
		20B	REV. FIGURE 6			PREPARED/APPROVED BY
		20C	REV. FIGURE 6			
	W	20D	REV. FIGURE 6			DRAWN BY / DETAILED BY
			MARK FRIEDRICH (313) 59-[illegible]			
[illegible]			PROD REL DRDO-E-[illegible]	[illegible]	[illegible]	
	X	11	REV FUNCTIONAL TESTS			
	X	12	REV FIGURE 5			
	X	20D	REV FIGURE 6			
	X	22	REV FIGURE 6			
			MARK FRIEDRICH (313) 59-07964	[illegible]		
[illegible]			DROO-E-1048[illegible]-002	CK	[illegible]	MANUFACTURING ENGR.
	Y	17 THRU 23	REVISED			
			MARK FRIEDRICH (313) 59-07964			QUALITY CONTROL
[illegible]			PROD REL DRDO-E-[illegible]	[illegible]	[illegible]	
	Z	ALL	[illegible]			PURCHASING
			M FRIEDRICH (313) 59-07964		[illegible]	
[illegible]			PROD RD. DRDO-E-[illegible]	[illegible]	[illegible]	SUPPLIER QUALITY ASSURANCE

PAGE 1C OF 53 REV Z

FORM [illegible]

3718 7259

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TABLE OF CONTENTS

TABLE OF CONTENTS
(continued)

TABLE OF CONTENTS
(continued)

TABLE OF CONTENTS
(continued)

TABLE OF FIGURES

1 GENERAL

This specification governs the speed control amplifier assembly. It is a subassembly to an electronic Speed Control system which regulates vehicle speed. The amplifier subassembly is comprised of a leadframe housing, aluminum baseplate, solid state electronic circuit and protective encapsulant.

This Engineering Specification is a supplement to the released drawing on the released part, and all requirements herein must be met in addition to all other requirements of the part drawing. Minimum measures necessary for demonstrating compliance to these requirements are given in each section.

The Engineering Specification is intended to evaluate specific characteristics as a supplement to normal material inspections, dimensional checking, and in-process controls, and should in no way adversely influence other inspection operations.

Preparation and submission of an acceptable Control Plan are the responsibility of the manufacturing source. Control Plan approval by the Component Engineering & Manufacturing Operations and by other activities according to QS-9000 is a prerequisite for initial sample review and approval. The manufacturing source will retain the original of the approved control plan and any later revisions per QS-9000 and provide a copy to the design responsible OEM.

2 PRODUCTION VALIDATION AND IN-PROCESS TESTS

Production Validation (PV) tests are used to obtain an initial estimate of the process potential to produce parts that conform to engineering requirements, and to identify causal or predictive relationships between significant design and process characteristics (to be used for process control). These tests must be completed satisfactorily using initial parts from production tooling and processes before Part Submission Warrant (PSW) approval and authorization of production parts can be issued. Sampling plans for PV testing must be included in the Control Plan.

In-process (IP) tests are used to further understand the relationship between significant design and process characteristics and to establish a basis for continuing improvement. Tests must be completed with production parts on an on-going basis. Sampling plans for both IP testing and evaluation of the significant process characteristics must be included in the Control Plan. When the process is found to be out of control or the test acceptance criteria are not met, the reaction plan approved in the Control Plan shall be invoked.

Figures 1 and 1a list the tests required for production validation (PV) and in-process (IP) testing. Refer to section 3.3 for descriptions of each test.

Figure 1 - Production Validation and In-Process Tests - Families C, F, G					
Test Number	Test Name	Use	Limits See Fig. 6	Minimum Conformance to Tolerance	Suggested Frequency / Sample Size *
3.3.1	Three Temperature Functional	PV/IP			5/
3.3.1.1	EMI Filter Capacitor	PV/IP		Cpk > 1.33	
3.3.1.2	Driver Command Bias Test	PV/IP		Cpk > 1.33	
3.3.1.3	Module Quiescent Current	PV/IP		Cpk > 1.33	
3.3.1.4	Software Version	PV/IP		1/	
3.3.1.5	Micro RAM, ROM, & A/D Conv. Tests	PV/IP		1/	
3.3.1.6	Resonator Test	PV/IP		Cpk > 1.33	
3.3.1.7	System Voltage A/D Test	PV/IP		2/	
3.3.1.8	Command Voltage A/D Test	PV/IP		2/	
3.3.1.9	Over Voltage Detector A/D Test	PV/IP		2/	
3.3.1.10	Deactivator Switch Threshold Test	PV/IP		1/	
3.3.1.11	Speed Sensor High Threshold Test	PV/IP		Cpk > 1.33	
3.3.1.12	Solenoid Sink Sat. Voltage Test	PV/IP		3/	
3.3.1.13	Speed Sensor Low Threshold Test	PV/IP		Cpk > 1.33	
3.3.1.14	Mtr. Driver Saturation Voltage Test	PV/IP		4/	
3.3.1.15	Set Indicator Saturation Test	PV/IP		3/	
3.3.1.16	Trans. Interface Saturation Test	PV/IP		3/	
3.3.1.17	Watchdog Timer Test	PV/IP		1/	
3.3.1.18	Trans. Interface Open Ckt Volt.	PV/IP		Cpk > 1.33	
3.3.1.19	Test	PV/IP		Cpk > 1.33	
3.3.1.20	Set Indicator Open Ckt Volt. Test	PV/IP		Cpk > 1.33	
3.3.1.21	Brake Pull-up Test	PV/IP		3/	
3.3.1.22	FET Leakage Test	PV/IP		Cpk > 1.33	
3.3.1.23	Deactivator Leakage Test	PV/IP		Cpk > 1.33	
3.3.1.24	FET Avalanche/Diode VF Test	PV/IP		1/	
3.3.1.25	Redundant Brake Test	PV/IP		1/	
	Brake Open Harness In. Ckt Test				
3.3.3	End-of-Line Tests	IP		Same as 3.3.1	100%
3.3.4	Reliability Monitoring	IP		1/	5/
3.4.3.14	EMC - ESD	PV		1/	2/Yr.
3.4.5.6	Thermal Shock Resistance	PV/IP		2/	18/Yr.
3.4.5.7	Thermal Shock Endurance	PV/IP		1/	6/Yr.
3.4.5.8	Humidity-Temperature Cycle	PV/IP		1/	18/Yr.
3.4.6.1.1	Vibration	PV/IP		1/	18/Yr.
3.4.6.3.2	Bench Drop	PV/IP		1/	18/Yr.

1/ GO / NO-GO Test - All Must Pass
2/ Digital resolution of module restricts statistical significance - all must pass.
3/ Capability to be within 3 SIGMA of upper tolerance limit.
4/ Test 0.1, 0.2, 0.3 to be within 3 SIGMA of upper tolerance limit; 0.4: Cpk > 1.33.
5/ Modules may be mixed generically for lot testing; see control plan. Subsequent families must be run in subsequent quarters.

* It is recommended that IP test sample sizes and frequencies be developed by the manufacturer, with concurrence by CEMD, and documented in the Control Plan.

Figure 1a - Production Validation and In-Process Tests - Family M

Test Number	Test Name	Use	Limits See Fig. 6	Minimum Conformance to Tolerance	Suggested Frequency / Sample Size *
3.3.2	Three Temperature Functional	PV/IP			5/
3.3.2.1	EMI Filter Capacitor	PV/IP		Cpk > 1.33	
3.3.2.2	Driver Command Bias Test	PV/IP		Cpk > 1.33	
3.3.2.3	Module Quiescent Current	PV/IP		Cpk > 1.33	
3.3.2.4	Software Version	PV/IP		1/	
3.3.2.5	Micro RAM, ROM, & A/D Conv. Tests	PV/IP		1/	
3.3.2.6	Resonator Test	PV/IP		Cpk > 1.33	
3.3.2.7	System Voltage A/D Test	PV/IP		2/	
3.3.2.8	Command Voltage A/D Test	PV/IP		2/	
3.3.2.9	Over Voltage Detector A/D Test	PV/IP		2/	
3.3.2.10	Deactivator Switch Threshold Test	PV/IP		1/	
3.3.2.11	ON/OFF Switch Threshold Test	PV/IP		1/	
3.3.2.12	2nd Command Switch Threshold Test	PV/IP		1/	
3.3.2.13	Speed Sensor Low Threshold Test	PV/IP		Cpk > 1.33	
3.3.2.14	Solenoid Sink Sat. Voltage Test	PV/IP		3/	
3.3.2.15	Speed Sensor High Threshold Test	PV/IP		Cpk > 1.33	
3.3.2.16	Mtr. Driver Saturation Voltage Test	PV/IP		4/	
3.3.2.17	Set Indicator Saturation Test	PV/IP		3/	
3.3.2.18	Trans. Interface Saturation Test	PV/IP		3/	
3.3.2.19	Watchdog Timer Test	PV/IP		1/	
3.3.2.20	Trans. Interface Open Ckt Volt.	PV/IP		Cpk > 1.33	
3.3.2.21	Test	PV/IP		Cpk > 1.33	
3.3.2.22	Set Indicator Open Ckt Volt. Test	PV/IP		Cpk > 1.33	
3.3.2.23	Brake Pull-up Test	PV/IP		3/	
3.3.2.24	FET Leakage Test	PV/IP		Cpk > 1.33	
3.3.2.25	Deactivator Leakage Test	PV/IP		Cpk > 1.33	
3.3.2.26	FET Avalanche/Diode V. Test	PV/IP		1/	
3.3.2.27	Redundant Brake Test	PV/IP		1/	
	Brake Open Harness Inhibit Test				
3.3.3	End-of-Line Tests	IP		Same as 3.3.2	100%
3.3.4	Reliability Monitoring	IP		1/	3/
3.4.3.13	EMC - ESD	PV		1/	2/Yr.
3.4.5.6	Thermal Shock Resistance	PV/IP		1/	16/Yr.
3.4.5.7	Thermal Shock Endurance	PV/IP		1/	6/Yr.
3.4.5.8	Humidity-Temperature Cycle	PV/IP		1/	16/Yr.
3.4.6.1.1	Vibration	PV/IP		1/	16/Yr.
3.4.6.3.3	Bench Drop	PV/IP		1/	16/Yr.

1/ GO / NO-GO Test - All Must Pass
2/ Digital resolution of module restricts statistical significance - all must pass.
3/ Capability to be within 3 SIGMA of upper tolerance limit.
4/ Test 0.1, 0.2, 0.3 to be within 3 SIGMA of upper tolerance limit; 0.4: Cpk > 1.33.
5/ Modules may be mixed generically for lot testing; see control plan. Subsequent families must be run in subsequent quarters.

* It is recommended that IP test sample sizes and frequencies be developed by the manufacturer, with concurrence by CEMO, and documented in the Control Plan.

3718 7266

FIGURE 3- PRODUCTION VALIDATION AUDIT TESTS / SEQUENCE						
TEST		TESTING SEQUENCE WITHIN THE SUBGROUP				SUGGESTED FREQUENCY
Ref. No. 1/ 2/	Title	SUB-GROUP A	SUB-GROUP B	SUB-GROUP C	SUB-GROUP D	
SAMPLE SIZE		[illegible]	SIX	THREE	TWELVE	
3.4.1.1.1/ 3.4.2.1.4	Performance/Functional Evaluations	1,3,7	1,3	1,3	1,3	Yearly
3.4.1.1.6	Inspections	8	4		4	Yearly
3.4.5.6	Thermal Shock Resistance	2				Yearly
3.4.6.1	Vibration					
3.4.6.1.1	Vibration Endurance (3)	4				Yearly
3.4.6.3	Mechanical Shock/Drop					
3.4.6.3.3	Bench Drop	5				Yearly
3.4.5.8	Humidity-Temperature Cycle 3/	6				Yearly
3.4.5.7	Thermal Shock Endurance		2			Yearly
3.4.3.14 2/	Electrostatic Discharge - Unpowered			2		Yearly
3.4.8.1	High-Temperature Endurance 3/				2	4/

1/ Reference: Electronic/Electro-Mechanical Test Methods ES-F2AF-1A[illegible]-AA
2/ For Electrical Environment Tests: Reference WSA [illegible] - ELECTRICAL REQUIREMENTS - Electrical/Electronic Components and Electromagnetic Compatibility Specification - ES-F2AF-1315-AA
3/ Power to Pins 7,8, Ground to pin 10, unmonitored.
4/ Not required for PV, informational purposes only as part of never-ending-improvement.

3718 7267

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3 TEST PROCEDURES AND REQUIREMENTS

3.1 General

Every Speed Control Module assembly or subassembly shall be capable of passing the Functional, Production Validation, In-process and End of Line Tests specified. Factory ambient tests shall be conducted at 25C +/-5C. In addition to all the tests specified herein, all amplifier module assemblies must pass the Speed Control Actuator final assembly (mechanical servo attached) specification ES-F2VF-9C735-AA.

The following operating conditions and environmental test classifications apply to this module, per the System Design Specification / Product Verification Specification. For definitions of each refer to the [illegible].

3.1.1 Operating Conditions

3.1.1.1 Environmental Test Classifications

Functional Importance Class (FIC)	A
Temperature Class	V
Vibration Class	II
Mechanical Shock/Drop Class	II

3.1.1.2 Temperature

Exposure Test	T5(min) = -40°C	T6(max) = 150°C *
Operation Test	T1(min) = -40°C	T2(max) = 115°C
Performance Test	T3(min) = -40°C	T4(max) = 125°C
Functional Test	T1(min) = -40°C	T7(max) = 125°C

* Prolonged storage above 100°C is not recommended. No short term damage will be apparent, however heat aging will accumulate.

3.1.1.3 Voltage

Normal	V1 = 11 volts	V2 = 16 volts
	V3 = 11 volts	V4 = 16 volts
Short Term (survive)		16 to 18 volts
Momentary (1 second)		18 to 24 volts
Abnormal Low (survive)		6 to 11 volts

3.1.1.4 Operational Life and Duty Cycle Ratings

Hours	8000
Miles	150,000

3 TEST PROCEDURES AND REQUIREMENTS (cont'd)

3.2 Test Setup / Test Conditions

Modules must meet this specification in the temperature range of -40°C to 125°C. Sample testing must be performed at -40°C, 25°C, and 125°C ambient. Unless the procedure itemized below is used, the environmental chamber soak time when performing functional tests at temperature extremes shall be 2 hours. This allows the servo to stabilize at the final test temperature for most chamber capacities and loading. The limiting factor being the chamber cooling capacity when fully loaded.

The soak time in the QC audit area may be reduced for three temperature functional testing if the time required to reach the temperature extremes, both hot and cold, is determined using a thermocouple type thermometer and a thermocoupled sample module. Procedure:

- Prepare a test sample module by drilling and tapping a #6-32 thread in an area of the module casting having the thickest cross section next to the motor. (This test sample should be saved for future use.)
- Using a #6-32 screw and washer, clamp a thermocouple under the washer firm against the module. (Alternate methods for attachment are not permitted).
- Load the chamber with the necessary fixtures, the maximum number of modules to be tested including the temperature verification module having the threaded hole in the casting and the thermocouple clamped using a screw and washer. Be sure the module containing the thermocouple is mounted at the station closest to the door.
- Record the time required for the verification module to stabilize within 2 degrees of final value.
- Take the stabilization times for hot and cold and adjust by multiplying each by 1.1 to account for unknown factors that will occur during normal testing.
- Use the adjusted time as the soak requirement. Post the soak time and date of validation and date of each revalidation on the front of the test equipment. Submit the adjusted soak times to CED.

The chamber soak time must be revalidated as follows:

- Every 6 months
- If any chamber service is done to correct a chamber problem,
- If the thermal loading of the chamber is increased (more things added to chamber since the last time Validated),
- If a different chamber is used.

3 TEST PROCEDURES AND REQUIREMENTS (cont'd)

3.3 Functional Evaluation Tests

The following tests are required for making a functional evaluation of this module as required by any of the environmental tests called out in section 3.4. Reference Figure 4 for the electrical test circuit. For Families C, F, G, (Base) reference Figure 5 for test circuit stimulus and Figure 6 for test limits. For Family H (Honda), reference Figure 5a for test circuit stimulus and Figure 6a for test limits. See Figure 11 for the Module Pinout Description. Not all tests are used on all families; see Figures 5, 5a, 6, 6a for details.

The tests have three categories: unpowered tests, monitor mode tests, and speed control mode tests.

3.3.1 Three Temperature Functional (-40, 25, 125°C) - Families C, F, G

Note: Tests 3.3.1.1.1 through 3.3.1.1.7 are run without power to the modules:

3.3.1.1 EMI Filter Capacitors

Measure the input capacitors at:

3.3.1.1.1 KEY IN RUN
3.3.1.1.2 SPEED SENSOR*
3.3.1.1.3 COMMAND SIGNAL
3.3.1.1.4 BRAKE INPUT
3.3.1.1.5 TRANSMISSION INTERFACE
3.3.1.1.6 INDICATOR OUTPUT
3.3.1.1.7 DEACTIVATOR SWITCH INPUT

- * To verify speed sensor capacitor, measure & record input impedance at a frequency of 1720 Hz.

Tests in the Monitor Mode (see Section 5.10):

Note: On reset, the module requires about 1 second to perform internal self tests on RAM, ROM, and A/D. After completion, for a period of three seconds, the module will permit wake up of the monitor. The monitor will stay awake if monitor commands are received at least every three seconds. If there are any system errors, the monitor aborts and speed control mode is entered. To save time after power up, perform tests 3.3.1.2 and 3.3.1.3 while the micro-controller is executing self tests, then start the monitor at test 3.3.1.4.

3.3.1.2 Driver Command Bias Test

3.3.1.2.1 Measure open circuit voltage at the COMMAND INPUT.
3.3.1.2.2 Measure short circuit current at the COMMAND INPUT.

3.3.1.3 Module Quiescent Current Test

With all external loads removed, measure the current draw of the module.

3 <u>TEST PROCEDURES AND REQUIREMENTS</u> (cont'd)

3.3 <u>Functional Evaluation Tests</u> (cont'd)

3.3.1 <u>Three Temperature Functional (-40, 23, 125°C) - Families G, F, E</u> (cont'd)

3.3.1.4 <u>Software Version</u>

Wake up the monitor and record the software version number.

3.3.1.5 <u>Micro RAM, ROM, and A/D Converter Tests</u>

Record a pass or fail number for these internal tests according to the following:

1 = Failed A/D
2 = Failed ROM
3 = Failed ROM and A/D
4 = Failed RAM
5 = Failed RAM and A/D
6 = Failed RAM and ROM
7 = Failed RAM, ROM, and A/D
8 = Passed IC Self Test

3.3.1.6 <u>Resonator Test</u>

Apply a speed signal at the SPEED SENSOR input. Fetch a two byte Speed value from RAM via the monitor and convert from hex to decimal. Calculate and record the resonator frequency using the equation below.

Resonator Frequency = (RAM value) X (Speed Signal Frequency) X 8

3.3.1.7 <u>System Voltage A/D Test</u>

Record the SYSTEM VOLTAGE A/D conversion via the monitor.

3.3.1.8 <u>Command Voltage A/D Test</u>

3.3.1.8.1 With the DRIVER COMMAND input open circuit, record the DRIVER COMMAND VOLTAGE A/D conversion via the monitor. Verify the balance of the DRIVER COMMAND conversion to the SYSTEM VOLTAGE conversion of test 3.3.1.7 by recording the difference between the two measurements of test 3.3.1.7 and 3.3.1.8.1.

Result = SYSTEM VOLTAGE conversion (test 3.3.1.7) - DRIVER COMMAND conversion (test 3.3.1.8.1)

3.3.1.8.2 Present a SET command to the DRIVER COMMAND input. Read the conversion and subtract the open circuit conversion from test 3.3.1.8.1.

Result = "SET" command conversion (test 3.3.1.8.2) - DRIVER COMMAND conversion (test 3.3.1.8.1)

3718 7271

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3 TEST PROCEDURES AND REQUIREMENTS (cont'd)

3.3 Functional Evaluation Tests (cont'd)

3.3.1 Three Temperature Functional (-40, 25, 125°C) - Families C, F, G (cont'd)

3.3.1.9 Over Voltage Test

Record the OVER VOLTAGE A/D conversion via the monitor.

3.3.1.10 Deactivator Switch Threshold

3.3.1.10.1 Set the DEACTIVATOR input to the high threshold, and read the deactivator input via the monitor.

3.3.1.10.2 Set the DEACTIVATOR input to the low threshold and read the deactivator input via the monitor.

3.3.1.11 Speed Sensor High Threshold Test

Apply a positive slope voltage ramp to the SPEED SENSOR input and record the voltage of the ramp the instant the SOLENOID SINK output switches from high to low.

3.3.1.12 Solenoid Sink Saturation Voltage Test

With the SOLENOID SINK output low, measure the output voltage.

3.3.1.13 Speed Sensor Low Threshold Test

Apply a negative slope voltage ramp to the SPEED SENSOR input and record the voltage of the ramp the instant the SOLENOID SINK output switches from low to high.

3.3.1.14 Motor Driver Saturation Voltage Test

3.3.1.14.1 Turn motor PHASE A on via monitor, measure the saturation voltage at PHASE A output, then turn motor PHASE A off via monitor.

3.3.1.14.2 Turn motor PHASE B on via monitor, measure the saturation voltage at PHASE B output, then turn motor PHASE B off via monitor.

3.3.1.14.3 Turn motor PHASE C on via monitor, measure the saturation voltage at PHASE C output.

3.3.1.14.4 With motor PHASE C on, measure the MOTOR DIODE forward voltage (Vf). Turn off PHASE C via monitor.

3.3.1.15 Set Indicator Saturation Test

Turn the INDICATOR on via monitor, measure the saturation voltage at the INDICATOR output, then turn INDICATOR off via monitor.

3.3.1.16 Transmission Interface Saturation Test

Record the voltage of the TRANSMISSION INTERFACE output.

3718 7272

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3 TEST PROCEDURES AND REQUIREMENTS (cont'd)

3.3 Functional Evaluation Tests (cont'd)

3.3.1 Three Temperature Functional (-40, 25, 125°C) - Families G, F, G (cont'd)

3.3.1.17 Watchdog Timer Test

Via the monitor, place the micro-controller in an endless loop causing the watchdog to time out. Record the time required for the TRANSMISSION INTERFACE to switch from high to low verifying a micro-controller reset.

NOTE: The remaining tests are performed in the speed control mode. Normally on reset the micro-controller performs a first set of internal self checks and on completion waits three seconds for wake up of the monitor. If no wake up occurs, speed control mode is entered requiring a second set of internal self tests. Testing time can be reduced if the following procedure is used.

- Immediately after watchdog reset, perform tests 3.3.1.18 through 3.3.1.21. Concurrently the micro-controller will take one second to perform internal self tests.
- Wake up the monitor and "jump" directly into the speed control mode eliminating the three second monitor time out.
- Perform test 3.3.1.22 while the internal speed filter reaches steady state, (requires 1.5 seconds).
- Finish the remainder of the tests.

3.3.1.18 Transmission Interface Open Circuit Voltage Test

Measure the open circuit voltage at the TRANSMISSION INTERFACE output.

3.3.1.19 Set Indicator Open Circuit Voltage Test

Measure the open circuit voltage at the SET INDICATOR output.

3.3.1.20 Brake Pull-up Test

Measure the open circuit voltage at the BRAKE input.

3.3.1.21 FET Leakage Test

3.3.1.21.1 Measure the leakage current at SOLENOID SINK
3.3.1.21.2 Measure the leakage current at PHASE A
3.3.1.21.3 Measure the leakage current at PHASE B
3.3.1.21.4 Measure the leakage current at PHASE C

3.3.1.22 Deactivator Leakage Test

Measure the leakage current at the DEACTIVATOR input.

3 TEST PROCEDURES AND REQUIREMENTS (cont'd)

3.3 Functional Evaluation Tests (cont'd)

3.3.1 Three Temperature Functional (-40, 25, 125°C) - Families E, F, G (cont'd)

3.3.1.23 FET Avalanche/Diode VF Test

3.3.1.23.1 Power amplifier through COMMAND SIGNAL input.
3.3.1.23.2 Open NOT IN RUN input.
3.3.1.23.3 Ground SOLENOID POWER.
3.3.1.23.4 Apply current at SOLENOID SINK, record VF.
3.3.1.23.5 Open SOLENOID power and record avalanche of SOLENOID SINK.
3.3.1.23.6 Ground MOTOR COMMON.
3.3.1.23.7 Apply current at PHASE A, record VF.
3.3.1.23.8 Open MOTOR COMMON & record avalanche of PHASE A.
3.3.1.23.9 Ground MOTOR COMMON.
3.3.1.23.10 Apply current at PHASE B, record VF.
3.3.1.23.11 Open MOTOR COMMON & record avalanche of PHASE B.
3.3.1.23.12 Ground MOTOR COMMON.
3.3.1.23.13 Apply current at PHASE C, record VF.
3.3.1.23.14 Open MOTOR COMMON & record avalanche of PHASE C.
3.3.1.23.15 Power amplifier through NOT IN RUN.
3.3.1.23.16 Open COMMAND SIGNAL input and dwell 100ms.

3.3.1.24 Redundant Brake Test

3.3.1.24.1 Apply speed and 100ms "ON" command at the COMMAND SIGNAL input.
3.3.1.24.2 Open circuit the COMMAND SIGNAL input for 100ms.
3.3.1.24.3 Apply a 100ms "OFF" command at the COMMAND SIGNAL input.
3.3.1.24.4 Open circuit the COMMAND SIGNAL input for 100ms and check that the SOLENOID SINK switches from high to low within max. time limit.
3.3.1.24.5 After the SOLENOID SINK switches from high to low, dwell 1.1s.
3.3.1.24.6 Reduce the speed frequency and check that the SOLENOID SINK switches high within the maximum time limit and remains high.

3.3.1.25 Brake Open Resume Inhibit Test

3.3.1.25.1 Apply speed, a 100ms "resume" command signal and check that the SOLENOID SINK switched from high to low with in the maximum time limit. The time duration of this step shall not exceed the maximum time limit.
3.3.1.25.2 Open the COMMAND SIGNAL input, apply brake and check that the SOLENOID SINK switches high within the maximum time limit and remains high.

3 TEST PROCEDURES AND REQUIREMENTS (cont'd)

3.3 Functional Evaluation Tests (cont'd)

3.3.2 Three Temperature Functional (-40, 25, 125°C) - Family [illegible]

Note: Tests 3.3.2.1.1 through 3.3.2.1.7 are run without power to the modules)

3.3.2.1 [illegible] Filter Capacitors

Measure the input capacitance at:

3.3.2.1.1 [illegible] IN RUN.
3.3.2.1.2 SPEED SENSOR*
3.3.2.1.3 COMMAND SIGNAL
3.3.2.1.4 BRAKE INPUT
3.3.2.1.5 TRANSMISSION [illegible]
3.3.2.1.6 SET-INDICATOR OUTPUT
3.3.2.1.7 DEACTIVATOR SWITCH INPUT
3.3.2.1.8 2nd COMMAND [illegible]
3.3.2.1.9 ON/OFF SWITCH INPUT

* To verify speed sensor capacitor, measure & record input impedance at a frequency of 1720 Hz.

Tests in the Monitor Mode (see Section 5.10):

Note: On reset, the module requires about 1 second to perform internal self tests on RAM, ROM, and A/D. After completion, for a period of three seconds, the module will permit wake up of the monitor. The monitor will stay awake if monitor commands are received at least every three seconds. If there are any system errors, the monitor aborts and speed control mode is entered. To save time after power up, perform tests 3.3.2.2 and 3.3.2.3 while the micro-controller is executing self tests, then start the monitor at test 3.3.2.4.

3.3.2.2 Driver Command Bias Test

3.3.1.2.1 Measure the open circuit voltage at the COMMAND INPUT.
3.3.1.2.2 Measure the short circuit current at the COMMAND INPUT.

3.3.2.3 Module Quiescent Current Test

With all external loads removed, measure the current draw of the module.

3.3.2.4 Software Version

Wake up the monitor and record the software version number.

3 TEST PROCEDURES AND REQUIREMENTS (cont'd)

3.3 Functional Evaluation Tests (cont'd)

3.3.2 Three Temperature Functional (-40, 25, 125°C) - Family [illegible] (cont'd)

3.3.2.5 Micro RAM, ROM, and A/D Converter Tests

Record a pass or fail number for these internal tests according to the following:

1 = Failed A/D
2 = Failed ROM
3 = Failed ROM and A/D
4 = Failed RAM
5 = Failed RAM and A/D
6 = Failed RAM and ROM
7 = Failed RAM, ROM, and A/D
8 = Passed IC Self Test

3.3.2.6 Resonator Test

Apply a speed signal at the SPEED SENSOR input. Fetch a two byte speed value from RAM via the monitor and convert from hex to decimal. Calculate and record the resonator frequency using the equation below.

Resonator Frequency = (RAM value) X (Speed Signal Frequency) X 8

3.3.2.7 System Voltage A/D Test

Record the SYSTEM VOLTAGE A/D conversion via the monitor.

3.3.2.8 Driver Command Ranges Test

3.3.2.8.1 With the DRIVER COMMAND input open, read the DRIVER COMMAND conversion via the monitor. Record the A/D conversion.

3.3.2.8.2 Set the DRIVER COMMAND input to Vignition. Read the conversion via the monitor. Record the A/D conversion.

3.3.2.8.3 Present a "SET" COMMAND to the DRIVER COMMAND input. Read the conversion via the monitor. Record the A/D conversion.

3.3.2.9 Over Voltage Test

Record the OVER VOLTAGE A/D conversion via the monitor.

3.3.2.10 Deactivator Switch Threshold

3.3.2.10.1 Set the DEACTIVATOR input to the high threshold, and read the deactivator input via the monitor.

3.3.2.10.2 Set the DEACTIVATOR input to the low threshold and read the deactivator input via the monitor.

3718 7276

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3 TEST PROCEDURES AND REQUIREMENTS (cont'd)

3.3 Functional Evaluation Tests (cont'd)

3.3.2 Three Temperature Functional (-40, 25, 125°C)- Family E (cont'd)

3.3.2.11 On/OFF Switch Input Test

3.3.2.11.1 Set ON/OFF input to Upper Threshold and record the ON/OFF input via the monitor.

3.3.2.11.2 Open ON/OFF input and record the ON/OFF input via the monitor.

3.3.2.12 Second Command Switch Input Test

3.3.2.12.1 Open SECOND COMMAND SWITCH input and record the SECOND COMMAND SWITCH input via the monitor.

3.3.2.12.2 Set SECOND COMMAND SWITCH input to Lower Threshold and record the SECOND COMMAND SWITCH input via the monitor.

3.3.2.12.3 Set SECOND COMMAND SWITCH input to Upper Threshold and record the SECOND COMMAND SWITCH input via the monitor.

(Note: Order of Tests 3.3.2.13 & 3.3.2.15 is opposite that of 3.3.1.11 & 3.3.1.13)

3.3.2.13 Speed Sensor Low Threshold Test

Apply Low Threshold Voltage to the SPEED SENSOR input and ensure the SOLENOID SINK output switches from high to low.

3.3.2.14 Solenoid Sink Saturation Voltage Test

With the SOLENOID SINK output low, measure the output voltage.

3.3.2.15 Speed Sensor High Threshold Test

Open circuit the SPEED SENSOR input and ensure the SOLENOID SINK output switches from low to high.

3.3.2.16 Motor Driver Saturation Voltage Test

3.3.2.16.1 Turn motor PHASE A on via monitor, measure the saturation voltage at PHASE A output, then turn motor PHASE A off via monitor.

3.3.2.16.2 Turn motor PHASE B on via monitor, measure the saturation voltage at PHASE B output, then turn motor PHASE B off via monitor.

3.3.2.16.3 Turn motor PHASE C on via monitor, measure the saturation voltage at PHASE C output.

3.3.2.16.4 With motor PHASE C on, measure the MOTOR DIODE forward voltage (VF). Turn off PHASE C via monitor.

3 <u>TEST PROCEDURES AND REQUIREMENTS</u> (cont'd)

3.3 <u>Functional Evaluation Tests</u> (cont'd)

3.3.2 <u>Three Temperature Functional (-40, 25, 125°C)- Family E</u> (cont'd)

3.3.2.17 <u>Set Indicator Saturation Test</u>

Turn the INDICATOR on via monitor, measure the saturation voltage at the INDICATOR output, then turn INDICATOR off via monitor.

3.3.2.18 <u>Transmission Interface Saturation Test</u>

Record the voltage of the TRANSMISSION INTERFACE output.

3.3.2.19 <u>Watchdog Timer Test</u>

Via the monitor, place the micro-controller in an endless loop causing the watchdog to time out. Record the time required for the TRANSMISSION INTERFACE to switch from high to low verifying a micro-controller reset.

NOTE: The remaining tests are performed in the speed control mode. Normally on reset the micro-controller performs a first set of internal self checks and on completion waits three seconds for wake up of the monitor. If no wake up occurs, speed control mode is entered requiring a second set of internal self tests. Testing time can be reduced if the following procedure is used.

- Immediately after watchdog reset, perform tests 3.3.2.20 through 3.3.2.23. Concurrently the micro-controller will take one second to perform internal self tests.
- Wake up the monitor and "jump" directly into the speed control mode eliminating the three second monitor time out.
- Perform test 3.3.2.23 while the internal speed filter reaches steady state, (requires 1.5 seconds).
- Finish the remainder of the tests.

3.3.2.20 <u>Transmission Interface Open Circuit Voltage Test</u>

Measure the open circuit voltage at the TRANSMISSION INTERFACE output.

3.3.2.21 <u>Set Indicator Open Circuit Voltage Test</u>

Measure the open circuit voltage at the SET INDICATOR output.

3.3.2.22 <u>Brake Pull-up Test</u>

Measure the open circuit voltage at the BRAKE input.

3.3.2.23 <u>FET Leakage Test</u>

3.3.1.21.1 Measure the leakage current at SOLENOID SINK
3.3.1.21.2 Measure the leakage current at PHASE A
3.3.1.21.3 Measure the leakage current at PHASE B
3.3.1.21.4 Measure the leakage current at PHASE C

[illegible]

Test	[illegible]	[illegible]	Type [illegible]			Type [illegible]			Type [illegible]			Type [illegible]			[illegible]
			[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	
[illegible] Filter Capacitors	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Driver Current Input	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible] Solenoid Current	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Software Version	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	
Micro Self Test	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
System Voltage	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	
Current Sense	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	
Overvoltage	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	
Trans. Switch Threshold	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	
Speed Sensor Threshold	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Solenoid Click Test	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Speed Sensor Threshold	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Output Driver Test	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Set Indicator Test	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Transmission Interface Test	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible] Timer	[illegible]	[illegible]			[illegible]			[illegible]			[illegible]			[illegible]	[illegible]

Figure 4 Functional Test Limits -40°C to 125°C

Test		Con.	Outputs	Amp Type B MIN	Amp Type B TARGET 25°C	Amp Type B MAX	Amp Type C MIN	Amp Type C TARGET 25°C	Amp Type C MAX	Amp Type F MIN	Amp Type F TARGET 25°C	Amp Type F MAX	
EMI Filter Capacitors	[illegible]	a.1	1-7	.71	.94	1.40	.71	.95	1.19	.71	.94	1.18	µF
	[illegible]	a.2	1-2	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
	[illegible]	a.3	1-3	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
	[illegible]	a.4	1-4	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
	[illegible]	a.5	1-5	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
	[illegible]	a.6	1-1	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
	[illegible]	a.7	1-9	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Driver Current Input		b.1 b.2	V 1-5 1-6 I 1-5	7.10 -16.36	7.41 -16.9	7.46 -17.5	7.10 -16.36	7.40 -16.9	7.46 -17.5	7.10 -16.35	7.41 -16.9	7.46 -17.5	V mA
Relay Solenoid Current		c	1 1-7	39.2	44.5	51.2	39.2	44.5	51.2	39.2	44.5	51.2	mA
Software Version		d	[illegible]	-	[illegible]	-	-	[illegible]	-	-	[illegible]	-	
Micro Self Test		e	[illegible]	-	P	-	-	P	-	-	P	-	
Resonator		f	[illegible]	[illegible]	4.000	[illegible]	[illegible]	4.000	[illegible]	[illegible]	4.000	[illegible]	[illegible]
System Voltage		g	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	
[illegible]	[illegible]	h.1 h.2	[illegible]	-4 [illegible]	0 [illegible]	4 [illegible]	-4 [illegible]	0 [illegible]	4 [illegible]	-4 [illegible]	0 [illegible]	4 [illegible]	
Overvoltage		i	[illegible]	46	[illegible]	[illegible]	46	[illegible]	[illegible]	46	[illegible]	[illegible]	
Sensor, Switch Threshold	[illegible]	j.1 j.2	[illegible]	- -	[illegible]	- -	- -	[illegible]	- -	- -	[illegible]	- -	
Speed Sensor Threshold	[illegible]	k	V 1-3 1-6	2.5	[illegible]	[illegible]	.3	.7	1.0	.3	.7	1.0	V
Solenoid [illegible] Test		l	V 3-2 1-10	40	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	40	[illegible]	[illegible]	[illegible]
Speed Sensor Threshold	[illegible]	m	V 1-5 1-6	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	V
Output Driver Test	[illegible]	n.1 n.2 n.3 n.4	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible] Indicator Test		o	V 1-1 1-6	[illegible]	[illegible]	2.7	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	V
Transmission Interface Out		p	V 1-2 1-6	-0.1	0.0	+0.2	-0.1	0.0	+0.2	-0.1	0.0	+0.2	V
Watchdog Timer		q	[illegible]			[illegible]			[illegible]			[illegible]	[illegible]

FIGURE 6 Functional Test Limits -40°C to 125°C

Test	Para.	Outputs	Amp Type [illegible] MIN	TARGET 25°C	MAX	Amp Type [illegible] MIN	TARGET 25°C	MAX	Amp Type [illegible] MIN	TARGET 25°C	MAX	Amp Type [illegible] MIN	TARGET 25°C	MAX	
EMI Filter Capacitors [illegible]	[illegible]	1-7 [illegible]	.71 [illegible]	.85 [illegible]	1.19 [illegible]	.71 [illegible]	.85 [illegible]	1.19 [illegible]	.71 [illegible]	.85 [illegible]	1.19 [illegible]	.71 [illegible]	.85 [illegible]	1.19 [illegible]	µF [illegible]
Driver Command Input	[illegible]	V 1-3 1-6 / I 1-5	7.10 / [illegible]	7.41 / [illegible]	7.46 / -17.5	7.10 / [illegible]	7.41 / [illegible]	7.46 / -17.5	7.10 / [illegible]	7.41 / [illegible]	7.46 / -17.5	7.10 / [illegible]	7.44 / [illegible]	7.46 / -17.5	V / mA
[illegible] Current	[illegible]	I 1-7	38.2	44.5	51.2	38.2	44.5	51.2	38.2	44.5	51.2	38.2	44.5	51.2	mA
Software Version	[illegible]	[illegible]	-	[illegible]	-	-	[illegible]	-	-	[illegible]	-	-	[illegible]	-	
Micro Self Test	[illegible]	[illegible]	-	P	-	-	P	-	-	P	-	-	P	-	
Resonator	[illegible]	[illegible]	[illegible]	4.000	[illegible]	[illegible]	4.000	[illegible]	[illegible]	4.000	[illegible]	[illegible]	4.000	[illegible]	[illegible]
System Voltage	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	
Current Levels [illegible]	[illegible]	[illegible]	-4 / [illegible]	0 / [illegible]	4 / [illegible]	-4 / [illegible]	0 / [illegible]	4 / [illegible]	-4 / [illegible]	0 / [illegible]	4 / [illegible]	-4 / [illegible]	0 / [illegible]	4 / [illegible]	
Overvoltage	[illegible]	[illegible]	44	50	[illegible]	44	50	[illegible]	44	50	[illegible]	44	50	[illegible]	
Trans. Switch Threshold [illegible]	[illegible]	[illegible]	- / -	1 / 0	- / -	- / -	1 / 0	- / -	- / -	1 / 0	- / -	- / -	1 / 0	- / -	
Speed Sensor Threshold [illegible]	[illegible]	V 1-3 1-6	-.3	.7	1.6	-.3	.7	1.6	2.5	[illegible]	[illegible]	-.3	.7	1.6	V
Solenoid Sink Test	[illegible]	V 2-3 1-10	40	100	250	40	100	250	40	100	250	40	100	250	[illegible]
Speed Sensor Threshold [illegible]	[illegible]	V 1-3 1-6	-1.06	-1.00	-.37	-1.06	-1.00	-.37	1.9	2.5	[illegible]	-1.06	-1.00	-.37	V
Output Driver Test [illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible] Indicator Test	[illegible]	V 1-1 1-6	2.2	[illegible]	2.7	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	V
Transmission Interface Test	[illegible]	V 1-2 1-6	-0.1	0.0	+0.2	-0.1	0.0	+0.2	-0.1	0.0	+0.2	-0.1	0.0	+0.2	V
Watchdog Timer	[illegible]	[illegible]			200			200			200			200	[illegible]

FIGURE 4 Functional Test Limits -40°C to 125°

TEST		[illegible]	Outputs	Amp Type 0 MIN	Amp Type 0 TARGET [illegible]°C	Amp Type 0 MAX	Amp Type 1 MIN	Amp Type 1 TARGET @ 25°C	Amp Type 1 MAX	
[illegible] Filter Capacitance	[illegible]	a.1	1-7	.71	.[illegible]	1.30	.7[illegible]	.[illegible]	1.[illegible]	µF
	[illegible]	a.2	1-[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	
	[illegible]	a.3	1-[illegible]	.[illegible]	.[illegible]	.[illegible]	.[illegible]	.[illegible]	.[illegible]	µF
	[illegible]	a.4	1-[illegible]	.[illegible]	.[illegible]	.[illegible]	.[illegible]	.[illegible]	.[illegible]	µF
	[illegible]	a.5	1-[illegible]	.[illegible]	.[illegible]	.[illegible]	.[illegible]	.[illegible]	.[illegible]	µF
	[illegible]	a.6	1-[illegible]	.[illegible]	.[illegible]	.[illegible]	.[illegible]	.[illegible]	.[illegible]	µF
	[illegible]	a.7	1-[illegible]	.[illegible]	.[illegible]	.[illegible]	.[illegible]	.[illegible]	.[illegible]	µF
Driver Control Input		b.1	[illegible] 1-6	7.10	7.4[illegible]	7.4[illegible]	7.10	7.4[illegible]	7.46	V
		b.2	[illegible]	-16.3[illegible]	-1[illegible]	-17.[illegible]	-16.3[illegible]	-1[illegible]	-17.[illegible]	mA
[illegible] Solenoid Current		c	[illegible] 1-7	3[illegible]	[illegible]	[illegible]	3[illegible]	[illegible]	[illegible]	mA
[illegible]		d	[illegible]	-	[illegible]	-	-	[illegible]	1	
[illegible] Self Test		e	[illegible]	-	P	-	-	P	-	
[illegible]		f	[illegible]	3.[illegible]	4.[illegible]	4.[illegible]	3.[illegible]	4.[illegible]	4.[illegible]	[illegible]
System Voltage		g	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	
[illegible]	[illegible]	h.1	[illegible]	-4	0	4	-4	0	4	
	[illegible]	h.2	[illegible]	-[illegible]	-[illegible]	-[illegible]	-[illegible]	-[illegible]	-[illegible]	
[illegible]		i	[illegible]	4[illegible]	5[illegible]	5[illegible]	4[illegible]	5[illegible]	5[illegible]	
[illegible] Switch	[illegible]	j.1	[illegible]	-	1	-	-	1	-	
Threshold	[illegible]	j.2	[illegible]	-	0	-	-	0	-	
Speed Sensor Threshold	[illegible]	k	[illegible] 1-3 1-6	.3	.7	1.0	.3	.7	1.0	
Solenoid [illegible] Test		l	[illegible] 1-10	4[illegible]	[illegible]	[illegible]	4[illegible]	[illegible]	[illegible]	[illegible]
Speed Sensor Threshold	[illegible]	m	[illegible] 1-3 1-6	-1.3[illegible]	-1.[illegible]	-.77	-1.3[illegible]	-1.[illegible]	-0.77	V
Output Driver Test	[illegible] A	n.1	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
	[illegible]	n.2	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
	[illegible] C	n.3	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
	[illegible]	n.4	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible] Indicator Test		o	[illegible] 1-6	[illegible]	[illegible]	[illegible]	.[illegible]	.[illegible]	.[illegible]	V
Transmission Interface Test		p	[illegible] 1-6	-0.1	0.0	+0.2	-0.1	0.0	+0.2	V
[illegible] Time		q	[illegible] 1-6			[illegible]	-	-	[illegible]	[illegible]

FIGURE 4 Functional Test Limits -40°C to 125°C

TEST		Para.	Outputs	Amp Types A: Min	Target 25°C	Max	Amp Types B: Min	Target 25°C	Max	Amp Types C: Min	Target 25°C	Max	
EMI Filter Capacitors	[illegible]	[illegible]	[illegible]	.71 [illegible]	.81 [illegible]	1.10 [illegible]	.71 [illegible]	.81 [illegible]	1.10 [illegible]	.71 [illegible]	.81 [illegible]	1.10 [illegible]	[illegible]
Driver Command Input		[illegible]	[illegible]	7.10 [illegible]	7.41 [illegible]	7.4[illegible] -17.5	7.10 [illegible]	7.41 [illegible]	7.4[illegible] -17.5	7.10 [illegible]	7.41 [illegible]	7.4[illegible] -17.5	[illegible]
[illegible] Current		[illegible]	[illegible]	39.2	44.5	[illegible]	[illegible]	44.5	[illegible]	[illegible]	44.5	[illegible]	[illegible]
Software Version		[illegible]	[illegible]	-	[illegible]	-	-	[illegible]	-	-	[illegible]	-	
Micro Self Test		[illegible]	[illegible]	-	P	-	-	P	-	-	P	-	
Resonator		[illegible]	[illegible]	[illegible]	4.000	[illegible]	[illegible]	4.000	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
System Voltage		[illegible]	[illegible]	175	[illegible]	[illegible]	175	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	
Command [illegible]	[illegible]	[illegible]	[illegible]	-4 [illegible]	0 [illegible]	4 [illegible]	-4 [illegible]	0 [illegible]	4 [illegible]	-4	0	4	
Overvoltage		[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	
[illegible] Threshold	[illegible]	[illegible]	[illegible]	-	[illegible]	-	-	[illegible]	-	-	[illegible]	-	
Speed Sensor Threshold	[illegible]	[illegible]	V 1-5 1-6	.3	.7	[illegible]	.5	.7	1.5	.3	.7	[illegible]	V
Solenoid Click Test		[illegible]	[illegible]	40	100	250	40	100	[illegible]	40	100	[illegible]	mV
Speed Sensor Threshold	[illegible]	[illegible]	V 1-5 1-6	-1.55	-1.00	-.27	[illegible]	[illegible]	-.37	[illegible]	[illegible]	-.27	V
Output Driver Test	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible] Indicator Test		[illegible]	V 1-1 1-6	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	V
Transmission Interface Test		p	V 1-2 1-6	-0.1	[illegible]	+0.2	-0.1	[illegible]	+0.2	0.1	[illegible]	0.2	V
Latching Timer		[illegible]	[illegible]			200			200			[illegible]	[illegible]

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3718 7263

3 TEST PROCEDURES AND REQUIREMENTS (cont'd)

3.3 Functional Evaluation Tests (cont'd)

3.3.2 Three Temperature Functional (-40, 25, 125°C) - Family X (cont'd)

3.3.2.24 Deactivator Leakage Test

Measure the leakage current at the DEACTIVATOR input.

3.3.2.25 FET Avalanche/Diode VF Test

3.3.2.25.1 Power amplifier through COMMAND SIGNAL input.
3.3.2.25.2 Open NOT IN RUN input.
3.3.2.25.3 Ground SOLENOID POWER.
3.3.2.25.4 Apply current at SOLENOID SINK, record VF.
3.3.2.25.5 Open SOLENOID power and record avalanche of SOLENOID SINK.
3.3.2.25.6 Ground MOTOR COMMON.
3.3.2.25.7 Apply current at PHASE A, record VF.
3.3.2.25.8 Open MOTOR COMMON & record avalanche of PHASE A.
3.3.2.25.9 Ground MOTOR COMMON.
3.3.2.25.10 Apply current at PHASE B, record VF.
3.3.2.25.11 Open MOTOR COMMON & record avalanche of PHASE B.
3.3.2.25.12 Ground MOTOR COMMON.
3.3.2.25.13 Apply current at PHASE C, record VF.
3.3.2.25.14 Open MOTOR COMMON & record avalanche of PHASE C.
3.3.2.25.15 Power amplifier through NOT IN RUN.
3.3.2.25.16 Open COMMAND SIGNAL input and dwell 100ms.

3.3.2.26 Redundant Brake Test

3.3.2.26.1 Apply speed and latch "ON" command at the ON/OFF switch input.
3.3.2.26.2 Apply a 150ms "SET" command at the COMMAND SIGNAL input (240 ohms to ground at COMMAND SIGNAL)
3.3.2.26.3 Open circuit the COMMAND SIGNAL input for 100 ms and check that the SOLENOID SINK switches from high to low within the maximum time limit.
3.3.2.26.4 After SOLENOID SINK switches from high to low, dwell for 1,100 ms.
3.3.2.26.5 Reduce the speed frequency and check that the SOLENOID SINK switches high within the maximum time limit and remains high.

3.3.2.27 Brake Open Harness Inhibit Test

3.3.2.27.1 Apply speed, a 100 ms "RESUME" command signal and check that the SOLENOID SINK switches from high to low within the maximum time limit. The time duration of this step shall not exceed the maximum time limit.
3.3.2.27.2 Open the COMMAND SIGNAL input, remove the brake load, and check that the SOLENOID SINK switches high within the maximum time limit and remains high.

[illegible] 4 (Cont.) Functional Test Limits -40°C to 85°C

Test		Test No.	Outputs	Amp Type: E MIN	Amp Type: E TARGET	Amp Type: E MAX	Amp Type: F MIN	Amp Type: F TARGET	Amp Type: F MAX	Amp Type: G MIN	Amp Type: G TARGET	Amp Type: G MAX	
Transmission Interface		[illegible]	[illegible]	[illegible]	5.10	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	V
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	11.40	[illegible]	[illegible]	[illegible]	[illegible]	V
Brake Pull-up		[illegible]	[illegible]	10.3	11.4	[illegible]	10.3	11.4	[illegible]	10.3	11.4	[illegible]	V
[illegible] Leakage	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible] Leakage		[illegible]	[illegible]	270	[illegible]	[illegible]	270	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	1.47	[illegible]	[illegible]	1.47	[illegible]	[illegible]	1.47	[illegible]	V
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Redundant Brake	[illegible]	[illegible]	[illegible]	-	-	[illegible]	-	-	[illegible]	-	-	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	-	-	[illegible]	-	-	[illegible]	-	-	[illegible]	[illegible]
Open Reverse Inhibit	[illegible]	[illegible]	[illegible]	-	-	[illegible]	-	-	[illegible]	-	-	[illegible]	[illegible]

*** Bold and underlined limits are values that differ from model type A.
**** All limits are listed for completeness.

FIGURE 6 (Cont.) Functional Test Limits [illegible]

[illegible]	Test No.	Outputs	Amp Type E Min	Amp Type E Target	Amp Type E Max	Amp Type J Min	Amp Type J Target	Amp Type J Max	Amp Type K Min	Amp Type K Target	Amp Type K Max	Amp Type L Min	Amp Type L Target	Amp Type L Max	
[illegible]	[illegible]	[illegible]	[illegible]	5.10	[illegible]	[illegible]	5.10	5.45	[illegible]	5.10	[illegible]	[illegible]	5.10	[illegible]	V
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	5.10	[illegible]	[illegible]	5.10	[illegible]	[illegible]	[illegible]	[illegible]	V
Brake Pull-up	[illegible]	[illegible]	10.3	11.4	12.5	10.3	11.4	12.5	10.3	11.4	12.5	10.3	11.4	12.5	V
[illegible] Leakage	[illegible]	[illegible]	-5	0	[illegible]	-5	0	[illegible]	-5	0	[illegible]	-5	0	[illegible]	µA
[illegible] Leakage	[illegible]	[illegible]	[illegible]	342	440	[illegible]	342	440	[illegible]	342	[illegible]	[illegible]	[illegible]	[illegible]	µA
[illegible]	[illegible]	[illegible]	[illegible]	1.47	[illegible]	[illegible]	1.47	[illegible]	[illegible]	1.47	[illegible]	[illegible]	1.47	[illegible]	V
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	-	-	[illegible]	-	-	[illegible]	-	-	[illegible]	-	-	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	-	-	[illegible]	-	-	[illegible]	-	-	[illegible]	-	-	[illegible]	[illegible]
Open [illegible]	[illegible]	[illegible]	-	-	[illegible]	-	-	[illegible]	-	-	[illegible]	-	-	[illegible]	[illegible]

*** [illegible]

**** [illegible]

3718 7286

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FIGURE 4 (Cont.) Functional Test Limits -40°C to 125°C

TEST		Test No.	Outputs	Amp Type B MIN	Amp Type B ROOM 25°C	Amp Type B MAX	Amp Type E MIN	Amp Type E ROOM 25°C	Amp Type E MAX	Amp Type F MIN	Amp Type F ROOM 25°C	Amp Type F MAX	
[illegible]		[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	V
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	V
Brake Pull-up		[illegible]	[illegible]	[illegible]	11.4	[illegible]	[illegible]	11.4	[illegible]	[illegible]	11.4	[illegible]	V
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]		[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	1.47	[illegible]	[illegible]	1.47	[illegible]	[illegible]	1.47	[illegible]	V
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

[illegible]
[illegible]

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ENGINEERING SPECIFICATION

[illegible] (Cont.) Functional Test Limits -40°C to 125°C

Test		Test Seq.	Outputs	Amp Type A Min	Amp Type A Target 25°C	Amp Type A Max	Amp Type B Min	Amp Type B Target 25°C	Amp Type B Max	Amp Type C Min	Amp Type C Target 25°C	Amp Type C Max	Amp Type D Min	Amp Type D Target 25°C	Amp Type D Max	
Transmission Interface		[illegible]	V 1-8 1-6	4.[illegible]	5.10	5.43	4.[illegible]	5.10	[illegible]	4.[illegible]	[illegible]	[illegible]	4.[illegible]	[illegible]	[illegible]	V
[illegible]	[illegible]	[illegible]	V 1-8 1-6	4.[illegible]	5.10	5.43	4.[illegible]	5.10	[illegible]	4.[illegible]	[illegible]	[illegible]	4.[illegible]	[illegible]	[illegible]	V
[illegible]		[illegible]	V 1-6 1-6	10.3	11.4	12.5	10.3	11.4	12.[illegible]	10.3	11.4	12.5	10.3	11.4	12.5	V
[illegible] Leakage	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible] Leakage		[illegible]	[illegible] 1-8	270	342	410	270	342	4[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	342	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	V [illegible]	1.[illegible]	1.47	1.[illegible]	1.[illegible]	1.47	1.[illegible]	1.[illegible]	1.47	1.[illegible]	1.[illegible]	1.47	1.[illegible]	V
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	-	-	[illegible]	-	-	[illegible]	-	-	[illegible]	-	-	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	-	-	[illegible]	-	-	[illegible]	-	-	[illegible]	-	-	[illegible]	[illegible]

Note: Bold and underlined limits are values that differ from model type A.
Note: All limits are listed for completeness.

3718 7288

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FIGURE 6 (Cont.) Functional Test Limits [illegible]

Test		Test Seq.	Outputs	Type [illegible] Min	Type [illegible] Target	Type [illegible] Max	Type [illegible] Min	Type [illegible] Target	Type [illegible] Max	
[illegible]		[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	V
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	V
[illegible]		[illegible]	[illegible]	[illegible]	11.4	[illegible]	[illegible]	11.4	[illegible]	V
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]		[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	1.47	[illegible]	[illegible]	1.47	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	-	-	[illegible]	-	-	[illegible]	[illegible]
	[illegible]	[illegible]	[illegible]	-	-	2000	-	-	2000	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	-	-	[illegible]	-	-	[illegible]	[illegible]

[illegible]

3 TEST PROCEDURES AND REQUIREMENTS (cont'd)

3.3 Functional Evaluation Tests (cont'd)

3.3.3 End of Line Test

End of line testing shall consist of all the functional evaluation tests described in 3.3.1 within 2 minutes after soak at 125C.

3.3.4 Reliability Monitoring

The modules will be subjected to the unpowered thermal shock process as defined by the plant and approved by the ACD-CHED Reliability monitoring is a daily audit where 12 modules/shift are tested in accordance with three temp. functional (3.3.1, 3.3.2) and 12 modules/shift thermal shocked five times then tested in accordance with three temp. functional (3.3.1,2) Shock temperature range is -40 C to +125 C with 30 min. hot soak and 30 min. cold soak. Total test time is 5 hours with a 2 chamber system.

3.4 Environmental Tests

Prior to durability testing the modules must be permanently marked as durability test units and must not be shipped for vehicle installation. Functional test data for every module must be saved prior to and after every durability test.

The following table lists the environmental tests required for Production Validation (PV) and In-Process (IP) testing. Refer to the indicated specifications for descriptions on how the tests are performed.

3718 7290

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3 TEST PROCEDURES AND REQUIREMENTS (cont'd)

3.4 Environmental Tests (cont'd)

FIGURE 3 - ENVIRONMENTAL TESTS			
TEST NUMBER	REFERENCE SPECIFICATION	MODULE CLASS	TEST
3.4.3.1A	ES-F2AF-1316-AA, Spec. - EMC Section 3.2.5 (also WSR 00.00EA-D07 Elec. Environ. Protection Sections 4.2 - 4.4)	A	3.4.3.1A - ELECTROSTATIC DISCHARGE - [illegible] 3 Discharges of +15 kV, -15 kV each. 1 Mohm to ground after each discharge
3.4.5.6	ES-F2AF-1A269-BA Section 3.4.5 Climatic Environment	V	3.4.5.6 - THERMAL SHOCK RESISTANCE TL=-40° C, TH=+125° C 6 cycles / 2 hour soak @ each temp. >10° C/min.
3.4.5.7		V	3.4.5.7 - THERMAL SHOCK ENDURANCE TL=-40° C, TH=+125° C 1000 cycles / 30 min soak @ each temp. >10° C/min.
3.4.5.8		V	3.4.5.8 - HUMIDITY/TEMPERATURE CYCLE 5 cycles per defined Time/Temp./Humidity Profile Humid Baseplate Up. NOTE: UNMONITORED, POWERED ONLY
3.4.6.1.1	ES-F2AF-1A269-BA Section 3.4.6 Mechanical Environment	II	3.4.6.1.1B - VIBRATION ENDURANCE Method (B)
3.4.6.3.3		IV	3.4.6.3.3 - BENCH DROP 30 cm per surface
3.4.8.1	ES-F2AF-1A269-BA Section 3.4.8 Demonstrated Life	N/A	3.4.8.1 - HIGH-TEMPERATURE ENDURANCE TL=115° C 1000 Hrs. at Temperature NOTE: UNMONITORED, POWERED ONLY

4 REVALIDATION REQUIREMENTS

Conditions requiring revalidation include changes in part design, material (or source), or manufacturing process that could affect part function, performance or durability.

The manufacturing source and the design responsible Product Engineering Office will jointly determine which potential changes to the process, materials or material sources would have significant impact on the product's function, performance, durability or appearance. The supplier will describe these conditions in the Control Plan, along with either

(1) the revalidation plan that would be followed in each case, or
(2) a provision to submit an amended Control Plan for approval if any of these process changes are planned.

The Control Plan must include a provision that, for any significant change in processing, ACP-CEMD and the manufacturing location (internal or supplier) shall jointly determine if PV re-testing is required, and if so, to what degree, i.e., Full or Mini PV.

No processing may be allowed without prior engineering approval of the process change and the attendant Control Plan changes.

5 INSTRUCTIONS AND NOTES

5.1. Control Plans

Control Plans address all significant design and process characteristics, which include all ES tests and Control Item characteristics. They describe the process potential studies that will be performed for product validation (including DV tests) and the ongoing product and process evaluation for continuing improvement (including IP tests). They include acceptance criteria, sample sizes, frequencies, data analysis methods and reaction plans.

The Control Plan is developed and updated as necessary by the manufacturing source in conjunction with the design responsible Component Engineering & Manufacturing Operations and other appropriate functions such as STA. The Control Plan defines the management of the upstream production process and part variables (significant process characteristics that affect the outcome of the ES tests or other significant design characteristics. The Control Plan also identifies the specific ES tests, with their sample sizes and frequencies, that will be performed in order to :

1. Confirm whether the process is being managed effectively.
2. Further identify significant process characteristics.
3. Evaluate performance of marginal processes.
4. Better anticipate the customer effect of the proposed process improvements.

For each part on which ES tests have been specified, the manufacturing source must present the Control Plan and any revisions to the design responsible Component Engineering & Manufacturing Operations for approval. This Component Engineering & Manufacturing Operations has flexibility to honor business relationships with suppliers having proprietary processes.

3718 7292

5 INSTRUCTIONS AND NOTES (cont'd)

5.2 Lot Definition

A lot consists of no more than eight hours of production per QS-9000.

5.3 Test Reporting and Record Retention

Recording and record retention shall conform to QS-9000. In addition:

5.3.1 Production Validation

All PV samples and the test results and data from production validation testing must be submitted in report form to ACD-CRMD prior to PSW. Component Engineering & Manufacturing Operations shall have final authority to approve PV testing.

5.3.2 In-Process

The IP test variable data produced as a result of performing the sample lot test requirements outlined in Section II must be collected and stored for ACD-CRMD review.

5.3.3 Test Report Contents

Equipment serial numbers, most recent date of calibration and test sample serial number must be recorded on all data sheets Test summaries must be sorted by test temperatures -40°C, 25°C or 125°C, and contain:

1) Sample Size
2) X - BAR
3) High Reading
4) Low Reading
5) Standard Deviation
6) Cp and Cpk
7) Upper Test Limit
8) Lower Test Limit

The records must be stored such that all parametric data for any one sample piece may be recalled with traceability to the lot in which the sample was taken.

5.3.4 Reporting Frequency

Once a month a summary of the reject rates for incoming inspection, line fallout, repair statistics, final test and audit tests, separated by part numbers and suppliers, shall be transmitted to ACD-CRMD and STA.

5.4 Test Correlation

Equipment calibration must be demonstrated at the beginning and middle of each shift by the supplier. Also, test equipment correlation between on-line and audit test equipment shall be performed by supplier. The procedure must be approved by ACD-CRMD and documented in the supplier control document.

5 INSTRUCTIONS AND NOTES (cont'd)

5.5 Fallout Analysis

5.5.1 In-Line Fallout

The assembly supplier is required to analyze all in-line fallout at the module level. All components from "isolated case" fallout and a sufficient quantity of "pattern" fallout must be analyzed to determine the root cause. All test methods and data used to identify the root cause will be submitted together with a report in an 8D format. Summary data of these results must be provided to ACD-[illegible] monthly.

5.5.2 Returns - Body & Assembly Division/Field

The supplier shall have the capability to analyze all returns and shall identify the root cause of the returns. A report for each identified root cause is to be delivered to ACD-[illegible] on a timely basis. All test methods and data used to identify the root cause will be submitted together with a report in an 8D format. Summary data of these results must be provided to ACD-[illegible] monthly.

5.6 Traceability

The manufacturer shall institute a traceability program per QS-9000 [illegible] for all components:

Housings, baseplates, adhesives, encapsulant, pastes, ceramics, ICs, transistors, diodes, resonators, resistors and capacitors.

In addition, each time a module is subjected to any of the following tests, the test, test results, (parametric data), and date tested shall be traceable from the clearly marked bar coded module serial number. The module serial number shall be contained in the bar code permanently marked on the module housing.

1. Daily IP Sample Tests 3.3.1
2. Daily Reliability Monitoring 3.3.4

5.7 Repairs

5.7.1 Definition

A repair is defined as the rework required for a module to pass a test requirement. The following restrictions apply.

a. A module may be repaired no more than a total of 3 times.
b. Excluding wire bonding and [illegible] applications, all repairs to the electronic circuit must be done before the substrate/PWB is mounted to the baseplate.
c. No component may be replaced more than once.
d. No wire bonding surface may be repaired more than once.
e. Any component which has been replaced during rework must be marked for visual identification.
f. Solder touch up to a given location may be done only once.
g. The substrate may not be reflowed on the reflow belt for repair.

5 [illegible] AND NOTES (cont'd)

5.5 Fallout Analysis

5.5.1 In-Line Fallout

The assembly supplier is required to analyze all in-line fallout at the module level. All components from "isolated case" fallout and a sufficient quantity of "pattern" fallout must be analyzed to determine the root cause. All test methods and data used to identify the root cause will be submitted together with a report in an 8D format. Summary data of these results must be provided to AED-[illegible] monthly.

5.5.2 Returns - Body & Assembly Division/Field

The supplier shall have the capability to analyze all returns and shall identify the root cause of the returns. A report for each identified root cause is to be delivered to AED-[illegible] on a timely basis. All test methods and data used to identify the root cause will be submitted together with a report in an 8D format. Summary data of these results must be provided to AED-[illegible] monthly.

5.6 Traceability

The manufacturer shall institute a traceability program per QS-9000 [illegible] for all components:

Housings, baseplates, adhesives, encapsulant, pastes, ceramics, ICs, transistors, diodes, resonators, resistors and capacitors.

In addition, each time a module is subjected to any of the following tests, the test, test results, (parametric data), and date tested shall be traceable from the clearly marked bar coded module serial number. The module serial number shall be contained in the bar code permanently marked on the module housing.

1. Daily IP Sample Tests 3.3.1
2. Daily Reliability Monitoring 3.3.4

5.7 Repairs

5.7.1 Definition

A repair is defined as the rework required for a module to pass a test requirement. The following restrictions apply.

a. A module may be repaired no more than a total of 3 times.
b. Excluding wire bonding and RTV applications, all repairs to the electronic circuit must be done before the substrate/PCB is mounted to the baseplate.
c. No component may be replaced more than once.
d. No wire bonding surface may be repaired more than once.
e. Any component which has been replaced during rework must be marked for visual identification.
f. Solder touch up to a given location may be done only once.
g. The substrate may not be reflowed on the reflow belt for repair.

5 INSTRUCTIONS AND NOTES (cont'd)

5.7 Repairs (cont'd)

5.7.2 Procedure

Repair of the modules may not be done until the manufacturers repair procedure is approved by ACD-CEMD.

The repair procedure must:

a. Identify the test station and report weekly results to the manufacturing Responsible engineer and be available to ACD-CEMD on request.
b. Define how the repair is to be performed for each component at each station reporting.
c. Define an acceptance standard to verify the repair was done to the proper component on the proper module.
d. Provide a method of identification and retrieval of the defective component part.
e. Identify the responsible party for investigating the defective component.

5.8 Packaging and Shipping

The packaging and shipment of parts must conform to the packaging and shipping guide, latest revision, as defined by the Material Handling Engineering Department, Manufacturing Engineering Office. The packaging must also be approved by ELD-PMD before PSW.

5.9 Other Engineering [illegible] Requirements

This section should be understood as an engineering requirement controlled by ACD-CEMD.

1. Equipment list for: PV, Lot Testing and IP Test Stations.

2. All procedures (i.e.., calibration, maintenance, equipment set up, station aids etc.) must be completed for production and IP test stations. The above procedures must be on display at all times or as specified by ELD-PMD.

3. An [illegible] tester handler must default to rejecting assemblies. The method must be approved by ACD-CEMD.

4. The PSW pilot run must be performed with the same methods and control documents and quality inspection as during production. ACD-CEMD must be informed of the pilot run one week prior and be allowed to observe.

5. The supplier must establish a key yield point weekly report form and submit the report to ACD-CEMD monthly or as requested.

5 [illegible] (cont'd)

5.10 SYSTEM MONITOR OPERATION - FAMILIES E, F, G, H

5.10.1 General

The system monitor is utilized by the Functional In-Process testers and Accelerated Life Testers for communication with the amplifier microcontroller. The communication is RS232.

5.10.2 Format and Configuration

The system monitor uses a synchronous serial communication interface in the microcontroller. Figure 11 illustrates the diagram of the system interface. For Families E,F,G and H (BASE and MAXMA), the RECEIVE DATA ([illegible]) line shares the Brake input pin (J1-4) and the TRANSMIT DATA OUT ([illegible]) line shares the Transmission Interface output pin (J1-2). The communication has the following format:

- A character has 1 start bit, 8 data bits, 1 stop bit, no parity.
- All characters are in uppercase ASCII format.
- Data is transmitted and received Least Significant Bit first.
- Transmission/Receive rate is 2400 baud.
- Memory and Data bytes are sent Most Significant Byte first.

5.10.3 Entering System Monitor (Sections 3.3.1.4, 3.3.2.4)

The system monitor is entered with the following sequence:

1. Apply power to the module.
2. Transmit an "M" to the module until the module replies with a ">" prompt. The power-up reset takes approximately 1 second.
3. Transmit a "[illegible]" as the 2 character password.
4. Once the password matches, the module will respond with a SOFTWARE VERSION LEVEL (1 byte that is 2 ASCII characters) and the result of the microcontroller's self-test ("P" = Pass, "F" = Fail, and the micro's RAM/ROM/A-D failure code).
5. The monitor routine is now activated and ready to receive instructions.

Once the monitor is active, it must receive a valid instruction character every 3 seconds. If a time-out occurs or an invalid instruction character is received, monitor mode will be aborted and the module will enter normal speed control mode. A JUMP instruction can be issued to keep the monitor from timing out.

5.10.4 System Monitor Commands

The system monitor routine will respond to three types of commands: Read, write, and jump. The following is the format for each command:

Command	Character Sent	Module Response			
READ	RAAAA	DD<CR>	AA,AAAA	=	address
WRITE	WAADD	<CR>	DD	=	data
PROGRAM	PAADD	<CR>	<CR>	=	carriage
JUMP	JAAAA	<CR>			return

3718 7297

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5 INSTRUCTIONS AND NOTES (cont'd)

5.10 SYSTEM MONITOR OPERATION - FAMILIES C, F, G, H

5.10.5 Functional Tests

Refer to Figures 8, 9 and 9a for addresses and port bit patterns, figures 10 and 10a for command examples.

A. Resonator Test: Perform two "READs" at the specified address. The most significant byte is read first. The value in Hexadecimal represents the micro timer count. Use the following equation to calculate the resonator frequency:

Frequency = (HEX value) X (Speed Signal Frequency) X 8

B. A/D Tests (System Voltage, Command Decode, Over Voltage Detector): These are analog inputs to the microcontroller. Use the following routine to decode the inputs:

- Perform a WRITE command to the specified memory location with the specified Channel number.
- Perform a JUMP to SUBROUTINE at the specified address.
- Perform a READ at the specified memory location to obtain the 8 bit result.

C. Reading/Writing to Digital Ports: To READ the Deactivator Switch Threshold, the Brake ON/OFF or 2nd Command Switch inputs, perform a READ instruction at the specified port address. The Motor Driver Phases A, B, C, Solenoid Sink, Transmission Interface, and Set Indicator outputs are turned ON or OFF by performing a write with bits 1 or 0 to the specified bit and port address.

D. Transmission Interface Saturation/Watchdog Timer Test: Turn SCI TDO off by performing a WRITE to the SCI control register in the micro to turn off the transmitter. Immediately following this instruction, there will be no more responses from the module for instruction inputs. Set the TRANSMISSION INTERFACE to OUTPUT by performing a WRITE to the specified Data Direction Register of the port. Turn on the TRANSMISSION interface by placing a 1 in the specified bit of the specified port using a WRITE instruction. Make a measurement of the TRANSMISSION SATURATION VOLTAGE at the specified module pin.

Perform a JUMP to the Watchdog subroutine, to allow the watchdog to time out and reset the microcontroller. The time it takes for the transmission output to switch from low to high indicates the watchdog timeout.

After Watchdog timeout reset, enter normal speed control mode by logging into monitor mode (5.10.3) and then perform a JUMP to the specified address to avoid the 3 second start-up.

6 COMPILATION OF REFERENCE DOCUMENTS

ES-F2VF-9A819-AA	HOUSING ASY-SPEED CONTROL ACTR
ES-F2VF-9C735-AA	SERVO ASSEMBLY SPEED CONTROL
ES-F2AF-1316-AA	ELECTROMAGNETIC COMPATIBILITY CONFORMANCE
ES-F2AF-1A263-AB	ELECTRONIC/ELECTRO-MECHANICAL ENVIRONMENTAL TEST METHODS
WDR00,00EA-D07	WORLDWIDE DESIGN REQUIREMENTS - ENVIRONMENTAL REQUIREMENTS (Vehicle electrical & electronic systems)
QS9000	QUALITY SYSTEMS REQUIREMENTS

NAA Form #1638, or approved equivalent

NAA Form #MED-9364 or approved equivalent

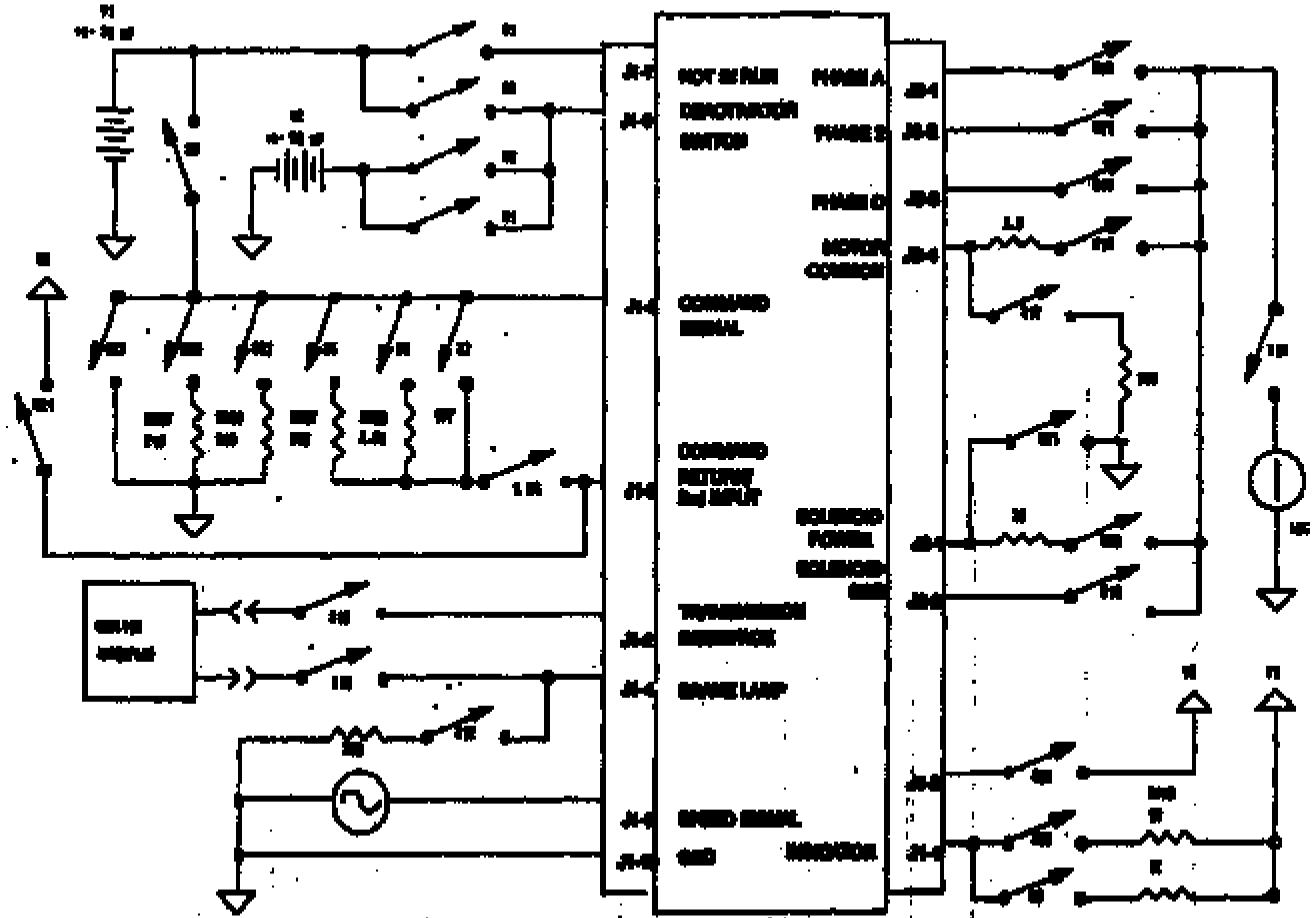
CONTINUING PROCESS CONTROL AND PROCESS CAPABILITY IMPROVEMENT, FMC

FORD RELIABILITY METHODS, FRM

PLANNING FOR QUALITY, FORD MOTOR COMPANY

FAP 3-1A5, SEC. VII, GUIDELINES FOR PART NUMBER IDENTIFICATION ON PARTS

NOTE: Outside suppliers should request all reference information from the Purchasing activity. Where necessary, Purchasing requests these documents from the affected Component Engineering & Manufacturing Operations.



FUNCTIONAL TEST DIAGRAM - NGSC BASE/OEM
FIGURE 4

[illegible] - Functional Test Selection and [illegible]

Test	Test No.	Columns 1–28	[illegible]	Outputs
[illegible] Filter Gap [illegible]	1.1	[illegible]	[illegible]	[illegible]
[illegible]	1.2	[illegible]	[illegible]	[illegible]
[illegible]	1.3	[illegible]	[illegible]	[illegible]
[illegible]	1.4	[illegible]	[illegible]	[illegible]
[illegible]	1.5	[illegible]	[illegible]	[illegible]
[illegible]	1.6	[illegible]	[illegible]	[illegible]
[illegible]	1.7	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Driver Command Input: OPEN CKT Voltage	2.1	[illegible]	[illegible]	[illegible]
Driver Command Input: SHORT CKT Current	2.2	[illegible]	[illegible]	[illegible]
[illegible] Solenoid Current	3	[illegible]	[illegible]	[illegible]
Software Version	4	[illegible]	[illegible]	[illegible]
Micro Self Test	5	[illegible]	[illegible]	[illegible]
[illegible]	6	[illegible]	[illegible]	[illegible]
Sensor Voltage A/D	7	[illegible]	[illegible]	[illegible]
Solenoid Voltage A/D [illegible]	8.1	[illegible]	[illegible]	[illegible]
[illegible]	8.2	[illegible]	[illegible]	[illegible]
Overvoltage Test	9	[illegible]	[illegible]	[illegible]
Comparator Threshold HI	10.1	[illegible]	[illegible]	[illegible]
Comparator Threshold LOW	10.2	[illegible]	[illegible]	[illegible]
Speed Sensor Threshold HI	11	[illegible]	[illegible]	[illegible]
Solenoid Sink Test	12	[illegible]	[illegible]	[illegible]
Speed Sensor Threshold LOW	13	[illegible]	[illegible]	[illegible]
[illegible] Connection [illegible]	14.1	[illegible]	[illegible]	[illegible]
[illegible]	14.2	[illegible]	[illegible]	[illegible]
[illegible]	14.3	[illegible]	[illegible]	[illegible]
[illegible]	14.4	[illegible]	[illegible]	[illegible]

Test	Test No.	Pins 01–28	V1 VB F I	Outputs
Indicator Test - Logic [illegible]	15	[illegible]	1 X 0 X	V 1-1 1-10
Indicator Test - Lamp [illegible]	15	[illegible]		
[illegible]	16	[illegible]	[illegible]	[illegible]
[illegible]	17	[illegible]	[illegible]	[illegible]
[illegible]	18	[illegible]	[illegible]	[illegible]
Indicator [illegible]	19	[illegible]	[illegible]	[illegible]
[illegible]	20	[illegible]	[illegible]	[illegible]
[illegible] Leakage	21-1 to 21-4	[illegible]	[illegible]	[illegible]
[illegible] Leakage	22	[illegible]	[illegible]	[illegible]
Diode [illegible] Clamp	23.1 [illegible]	[illegible]	[illegible]	[illegible]
Diode [illegible] Clamp	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

[illegible]			
[illegible]	[illegible]	[illegible] 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]

Function Generator [illegible]			
F Code	[illegible]	[illegible]	[illegible]
[illegible]	[illegible] volts [illegible] + ramp from [illegible] - ramp from [illegible] [illegible]	[illegible] volts [illegible] + ramp from [illegible] - ramp from [illegible] [illegible]	[illegible] volts [illegible] + ramp from [illegible] - ramp from [illegible] [illegible]

Current [illegible]		Voltage [illegible]		
I Code		V Code	V1	V2
[illegible]	don't care [illegible]	[illegible]	don't care [illegible] volts [illegible] volts	don't care [illegible] volts [illegible] volts

ENGINEERING SPECIFICATION

PART NUMBER [illegible]

Test	Test No.	01	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	[illegible]	[illegible]	[illegible]	[illegible]	Outputs
EMI Filter Caps																																		
[illegible]	1.1	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	1.2	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	1.3	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	1.4	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	1.5	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	1.6	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	1.7	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	1.8	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	1.9	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Driver Command Input																																		
OPEN CKT Voltage	2.1	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
SHORT CKT current	2.2	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	3	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Software Version	4	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Micro Self Test	5	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	6	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Output Voltage A/D	7	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Command Volt. A/D																																		
[illegible]	8.1	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	8.2	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	8.3	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible] Test	9	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible] Threshold																																		
[illegible]	10.1	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	10.2	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
On/Off Switch																																		
[illegible]	11.1	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	11.2	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
2nd Command Switch																																		
[illegible]	12.1	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	12.2	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	12.3	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Speed Sensor Threshold	13	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Solenoid Stick Test	14	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

ENGINEERING SPECIFICATION

TABLE [illegible] - Functional Test Selection and Measurement Values - [illegible]

Test	Test No.	Pins 01–28	V1 V2 F S	Outputs
Speed Sensor Threshold	15	[illegible]	[illegible]	[illegible]
Motor FET Saturation: Phase A / Phase B / Phase C / [illegible]	16.1 / 16.2 / 16.3 / 16.4	[illegible]	[illegible]	[illegible]
Gas Indicator Test	17	[illegible]	[illegible]	[illegible]
Transmission Test	18	[illegible]	[illegible]	[illegible]
Shutdown Timing	19	[illegible]	[illegible]	[illegible]
Transmission Open Ckt	20	[illegible]	[illegible]	[illegible]
Indicator Open Ckt	21	[illegible]	[illegible]	[illegible]
Brake Pull-up Test	22	[illegible]	[illegible]	[illegible]
Motor FET Leakage: Phase A / Phase B / Phase C / Solenoid	23.1 / 23.2 / 23.3 / 23.4	[illegible]	[illegible]	[illegible]
[illegible] Leakage	24	[illegible]	[illegible]	[illegible]
Diode V1/FET Clamp	25.1 – [illegible]	[illegible]	[illegible]	[illegible]

ENGINEERING SPECIFICATION

PART NUMBER [illegible]

3718 7306

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[illegible]	[illegible]	[illegible]	[illegible]

[illegible]	[illegible]	[illegible]

[illegible]			Group [illegible]			Group [illegible]			Group [illegible]			
Test	No.	[illegible]	Min	Target	Max	Min	Target	Max	Min	Target	Max	Unit
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	7.41 [illegible]	[illegible]	[illegible]	7.41 [illegible]	[illegible]	[illegible]	7.41 [illegible]	[illegible]	volts [illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Software Version	[illegible]	[illegible]		See Fig. 7			See Fig. 7			See Fig. 7		
[illegible]	[illegible]	[illegible]	-	[illegible]	-	-	[illegible]	-	-	[illegible]	-	
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	volts
[illegible]	[illegible]	[illegible]	[illegible]	1 [illegible]	[illegible]	[illegible]	1 [illegible]	[illegible]	[illegible]	1 [illegible]	[illegible]	volts volts
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	volts
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	volts volts
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	volts
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	volts
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	volts
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
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[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	3.3.1.[illegible]	[illegible]	-0.1	[illegible]	[illegible]	-0.1	[illegible]	[illegible]	-0.1	[illegible]	[illegible]	volts
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[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	-	-	[illegible]	-	-	[illegible]	-	-	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	-	-	[illegible]	-	-	[illegible]	-	-	[illegible]	[illegible]

3718 7306

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[illegible]												
			[illegible]			[illegible]			[illegible]			
Test	No.	Outputs	Min	Target	Max	Min	Target	Max	Min	Target	Max	Units
RFI Filter Caps [illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Driver Current Sine Test [illegible]	[illegible]	[illegible]	7.10 [illegible]	7.41 [illegible]	7.46 [illegible]	7.10 [illegible]	7.41 [illegible]	7.46 [illegible]	7.10 [illegible]	7.46 [illegible]	[illegible]	volts [illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Software Version	[illegible]	[illegible]		See Fig. 7			See Fig. 7			See Fig. 7		
[illegible]	[illegible]	[illegible]	-	[illegible]	-	-	[illegible]	-	-	[illegible]	-	
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
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[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Speed Sensor Low Thres.	[illegible]	[illegible]	[illegible]	[illegible]	4.7	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Motor PWM [illegible]	[illegible]	[illegible]	[illegible]	[illegible]	1100 [illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	3.7	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

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